4GB/8GB LPDDR5 SDRAM

VNL5E1024M32M-64S
VNL5E2048M32M-64S

Mobile LPDDR5 SDRAM

JLC4GPB-SM6, JLC8GPB-SM6

Features

- **Architecture**
  - 12.8 GB/s maximum bandwidth per channel
  - Frequency range: 800–5 MHz (data rate range per pin: 6400–40 Mb/s with WCK:CK = 4:1)
  - Selectable CKR (WCK:CK = 2:1 or 4:1)
- **LPDDR5 data interface**
  - Single x16 channel/die
  - Double-data-rate command/address entry
  - Differential command clocks (CK_t/CK_c) for high-speed operation
  - Differential data clocks (WCK_t/WCK_c)
  - Optional differential read strobe (RDQS_t/RDQS_c)
  - 16*n*-bit or 32*n*-bit prefetch architecture
  - Bank Architecture: 8-bank (8B) mode, bank group (BG) mode, and 16-bank (16B) mode supported
  - Command-selectable burst lengths (BL = 16 or 32) in bank group or 16-bank modes
  - Background ZQ calibration/command-based ZQ calibration
  - Optional link protection (linkECC)
  - Partial-array self refresh (PASR) and partial-array auto refresh (PAAR) with segment mask
- **Ultra-low-voltage core and I/Opower supplies**
  - V_{DD1} = 1.70–1.95V; 1.8V NOM
  - V_{DD2H} = 1.01–1.12V; 1.05V NOM
  - V_{DD2L} = V_{DD2H}or 0.87–0.97V; 0.9V NOM
  - V_{DDQ} = 0.5VNOM or 0.3V NOM (ODT off)
- **I/O characteristics**
  - Interface-LVSTL 0.5/0.3
  - I/O type: Low-swing single-ended, Vss terminated
  - V_{OH}-compensated output drive
  - Programmable Vss on-die termination (ODT)
  - Non target ODT support
  - DVFSQ support
- **Low power features**
  - DVFSC: Dynamic voltage frequency scaling core
  - Single-ended CK, single-ended WCK and single-ended RDQS
  - Data copy
  - Write X

Options

Marking

- V_{DD1}/V_{DD2H}/V_{DD2L}/V_{DDQ} (ODT on)/ (ODT off): 1.8V/1.05V/0.9V/0.5V/0.3V
- Array configuration
  - 1 Gig x 32 (2 channels x16 I/O) — 1024M32
  - 2 Gig x 32 (2 channels x16 I/O) — 2048M32
- Device configuration
  - 1G16 × 2 die in package — 1024M32
  - 1G16 × 4 die in package — 2048M32
- FBGA "green" package
  - 315-ball TFBGA
    12.4mm × 15.0mm,
    seated height 1.1mm (MAX)
- Speed grade, cycle time (tWCK)
  - 6400 Mb/s
- I_{DD} grade definition
  - Grade 1
- Operating temperature:
  - –25°C to +85°C
- Revision

Part Number Ordering Information

Table 1: **Ordering Information**

Organization	Density	Max Frequency	Part No.	Package
1024M*32	4GB(32Gb)	LPDDR5-6400Mbps	VNL5E1024M32M-64S	315 FBGA
2048M*32	8GB(64Gb)	LPDDR5-6400Mbps	VNL5E2048M32M-64S	315 FBGA

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Barycn FBGA part marking decoder is available at www.barycn,com

LPDDR5/LPDDR5X Data Sheet List

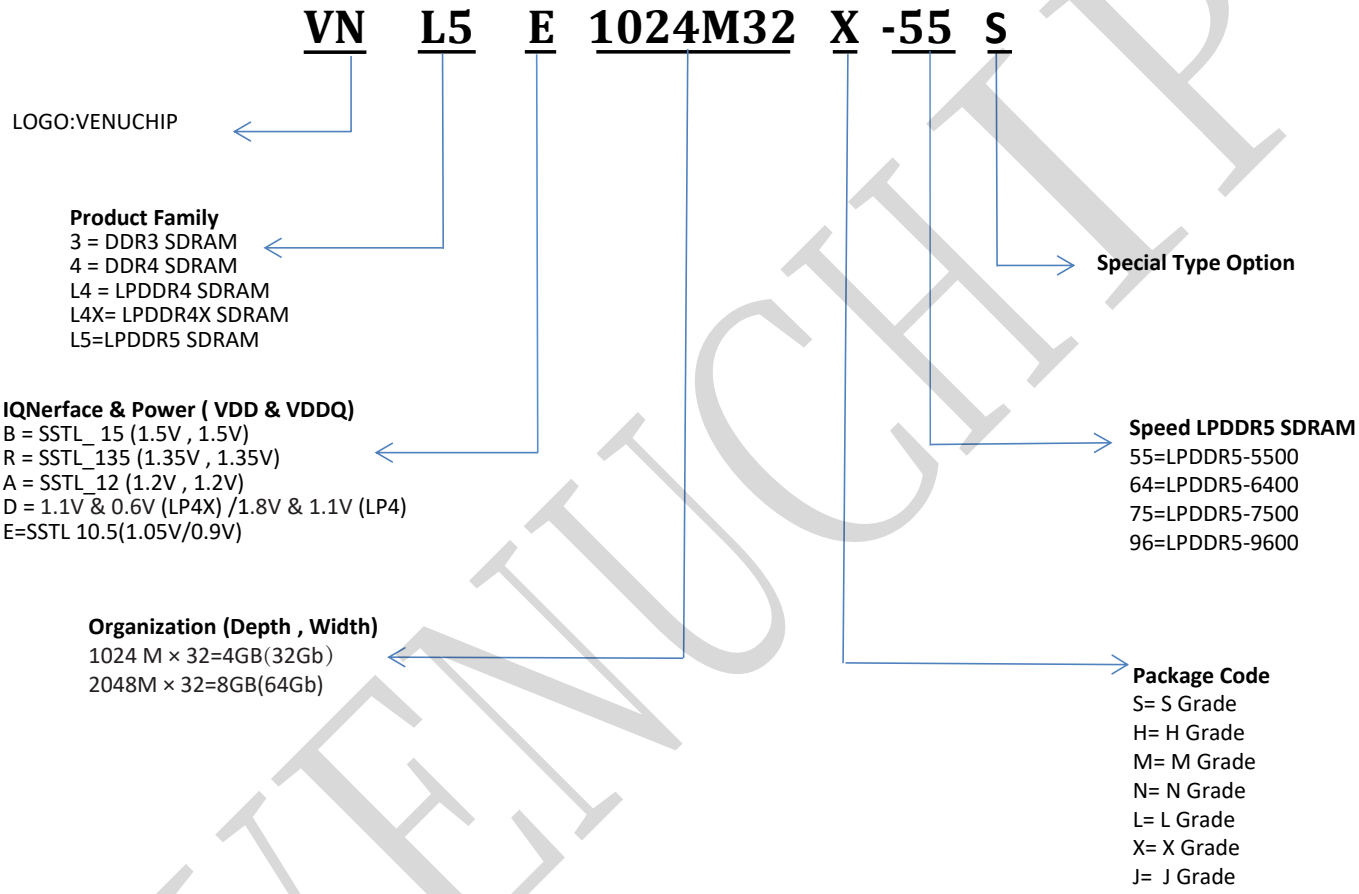
This data sheet only describes the product specifications that are unique to theBarycn devices listed in Table 1.

For general LPDDR5/LPDDR5X specifications, please refer to the data sheets below.

- General LPDDR5/LPDDR5X Specifications 1: Mode Registers
- General LPDDR5/LPDDR5X Specifications 2: AC/DC and Interface Specifications
- General LPDDR5/LPDDR5X Specifications 3: Features and Functionalities

1. Part Numbering Information

Venuchip Component Part Numbering Guide



Important Notes and Warnings

Barycn Technology, Inc. ("Barycn") reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions. This document supersedes and replaces all information supplied prior to the publication hereof. You may not rely on any information set forth in this document if you obtain the product described herein from any unauthorized distributor or other source not authorized by Barycn.

Automotive Applications. Products are not designed or intended for use in automotive applications unless specifically designated by Barycn as automotive-grade by their respective data sheets. Distributor and customer/distributor shall assume the sole risk and liability for and shall indemnify and hold Barycn harmless against all claims, costs, damages, and expenses and reasonable attorneys' fees arising out of, directly or indirectly, any claim of product liability, personal injury, death, or property damage resulting directly or indirectly from any use of non-automotive-grade products in automotive applications. Customer/distributor shall ensure that the terms and conditions of sale between customer/distributor and any customer of distributor/customer (1) state that Barycn products are not designed or intended for use in automotive applications unless specifically designated by Barycn as automotive-grade by their respective data sheets and (2) require such customer of distributor/customer to indemnify and hold Barycn harmless against all claims, costs, damages, and expenses and reasonable attorneys' fees arising out of, directly or indirectly, any claim of product liability, personal injury, death, or property damage resulting from any use of non-automotive-grade products in automotive applications.

Critical Applications. Products are not authorized for use in applications in which failure of the Barycn component could result, directly or indirectly in death, personal injury, or severe property or environmental damage ("Critical Applications"). Customer must protect against death, personal injury, and severe property and environmental damage by incorporating safety design measures into customer's applications to ensure that failure of the Barycn component will not result in such harms. Should customer or distributor purchase, use, or sell any Barycn component for any critical application, customer and distributor shall indemnify and hold harmless Barycn and its subsidiaries, subcontractors, and affiliates and the directors, officers, and employees of each against all claims, costs, damages, and expenses and reasonable attorneys' fees arising out of, directly or indirectly, any claim of product liability, personal injury, or death arising in any way out of such critical application, whether or Barycn or its subsidiaries, subcontractors, or affiliates were negligent in the design, manufacture, or warning of the Barycn product.

Customer Responsibility. Customers are responsible for the design, manufacture, and operation of their systems, applications, and products using Barycn products. Customers must ensure that adequate design, manufacturing, and operating safeguards are included in customer's applications and products to eliminate the risk that personal injury, death, or severe property or envi- ronmental damages will result from failure of any semiconductor component.

Limited Warranty. In no event shall Barycn be liable for any indirect, incidental, punitive, special or consequential damages (including without limitation lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort, warranty, breach of contract or other legal theory, unless explicitly stated in a written agreement executed by Barycn duly authorized representative.

General Notes

Throughout the data sheet, figures and text refer to DQs as DQ. DQ should be interpreted as any or all DQs collectively, unless specifically stated otherwise.

RDQS, CK, and WCK should be interpreted as RDQS_t, RDQS_c, CK_t, CK_c, and WCK_t, WCK_c respectively unless specifically stated otherwise. CA includes all CApins used for a given density.

In timing diagrams, CMD is used as an indicator only. Actual signals occur on CA[6:0].

V_{REF} indicates $V_{REF(CA)}$ and $V_{REF(DQ)}$.

Complete functionality is described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

Device Configuration

Table 2: Die Organization in the Package

Die Organization	1G32 (32 Gb/package)	2G32 (64 Gb/package)
Channel A, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel B, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel A, rank 1	–	x16 mode × 1 die
Channel B, rank 1	–	x16 mode × 1 die

Note: 1. Refer to the Package Block Diagram section in this data sheet.

Table 3: Die Addressing

Description	1G32 (32 Gb/package)/2G32 (64 Gb/package)		
Density per die	16Gb		
Bits	17,179,869,184		
Bank mode	BG mode	16B mode	8B mode
Configuration	64Mb × 16 DQ × 4 Banks × 4BG	64Mb × 16 DQ × 16 Banks	128Mb × 16 DQ × 8 Banks
Number of banks	4	16	8
Number of bank groups	4	1	1
Array prefetch bits	256	256	512
Rows per bank	65,536		
Columns	64		
Page size (bytes)	2048	2048	4096
Native burst length	16	16	32
Number of I/Os	16		
Bank address	BA[1:0]	BA[3:0]	BA[2:0]
Bank group address	BG[1:0]	–	–
Row address	R[15:0]		
Column address	C[5:0]		
Burst address	B[3:0]	B[3:0]	B[4:0]
Burst starting address boundary	128-bit		

Note: 1. Refer to the SDRAM Addressing section in General LPDDR5/LPDDR5X Specifications 3.

Refresh Requirement Parameters

Table 4: Refresh Requirement Parameters

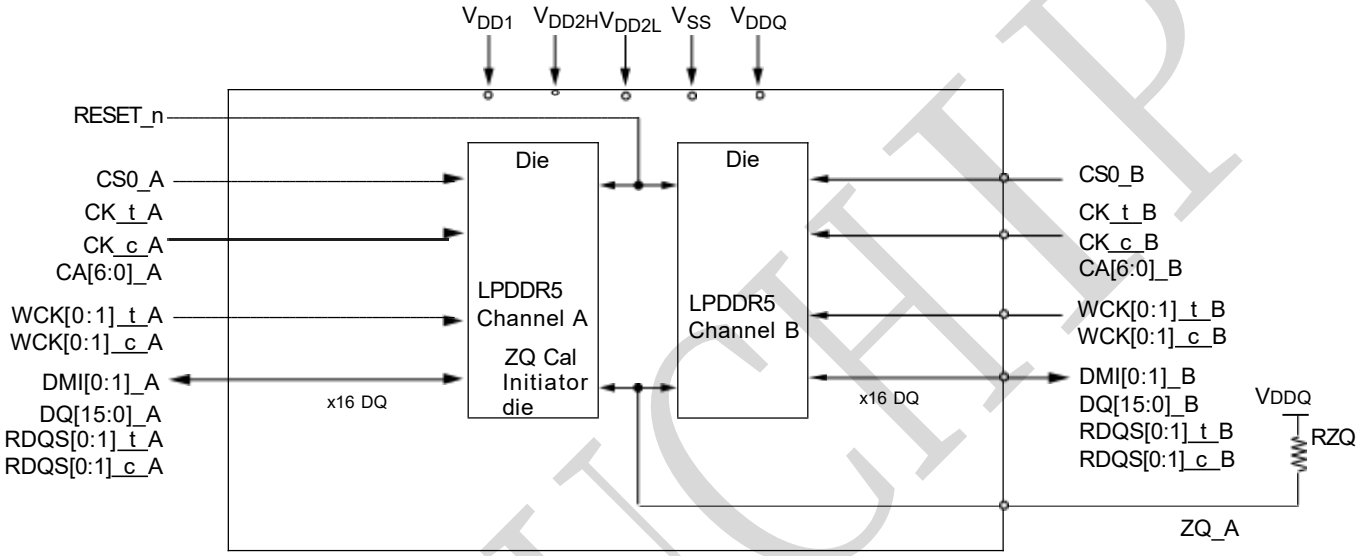
Parameter	Symbol	16Gb Die		Unit
		BG and 16B Mode	8B Mode	
REFRESH cycle time (all banks)	tRFCab	280	280	ns
REFRESH cycle time (per bank)	tRFCpb	140	140	ns
Per bank refresh to per bank refresh time (different bank)	tPBR2PBR	90	90	ns
Per bank refresh to ACTIVATE command time (different bank)	tPBR2ACT	7.5	10	ns

Note: 1. This table only describes refresh parameters that are density dependent. Refer to Refresh Requirement section in General LPDDR5/LPDDR5X Specifications 3 for all refresh parameters.

Package Block Diagrams

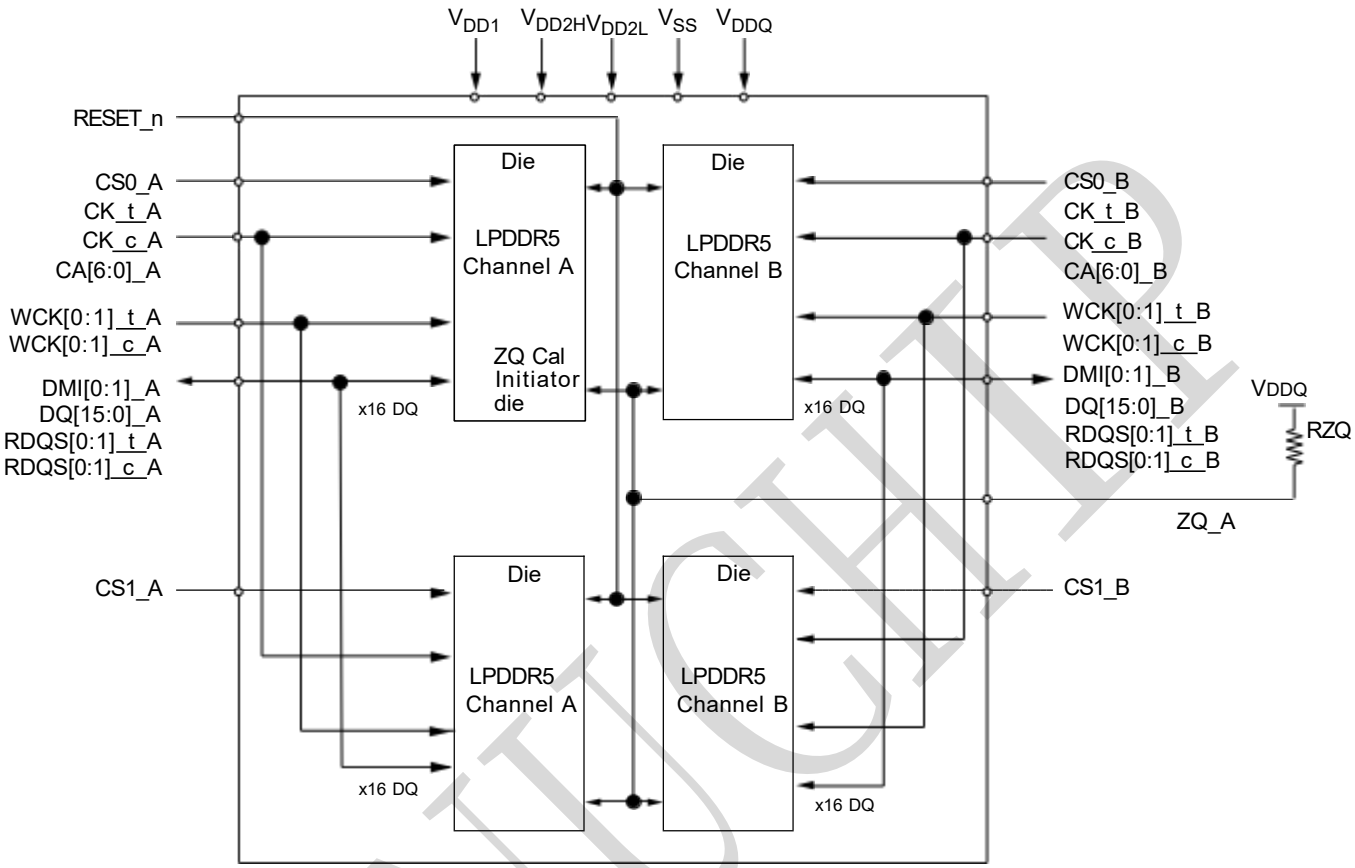
Dual Die, Dual Channel, Single Rank

Figure 2: Dual-Die, Dual-Channel, Single-Rank Package Block Diagram



Quad Die, Dual Channel, Dual Rank

Figure 3: Quad-Die, Dual-Channel, Dual-Rank Package Block Diagram



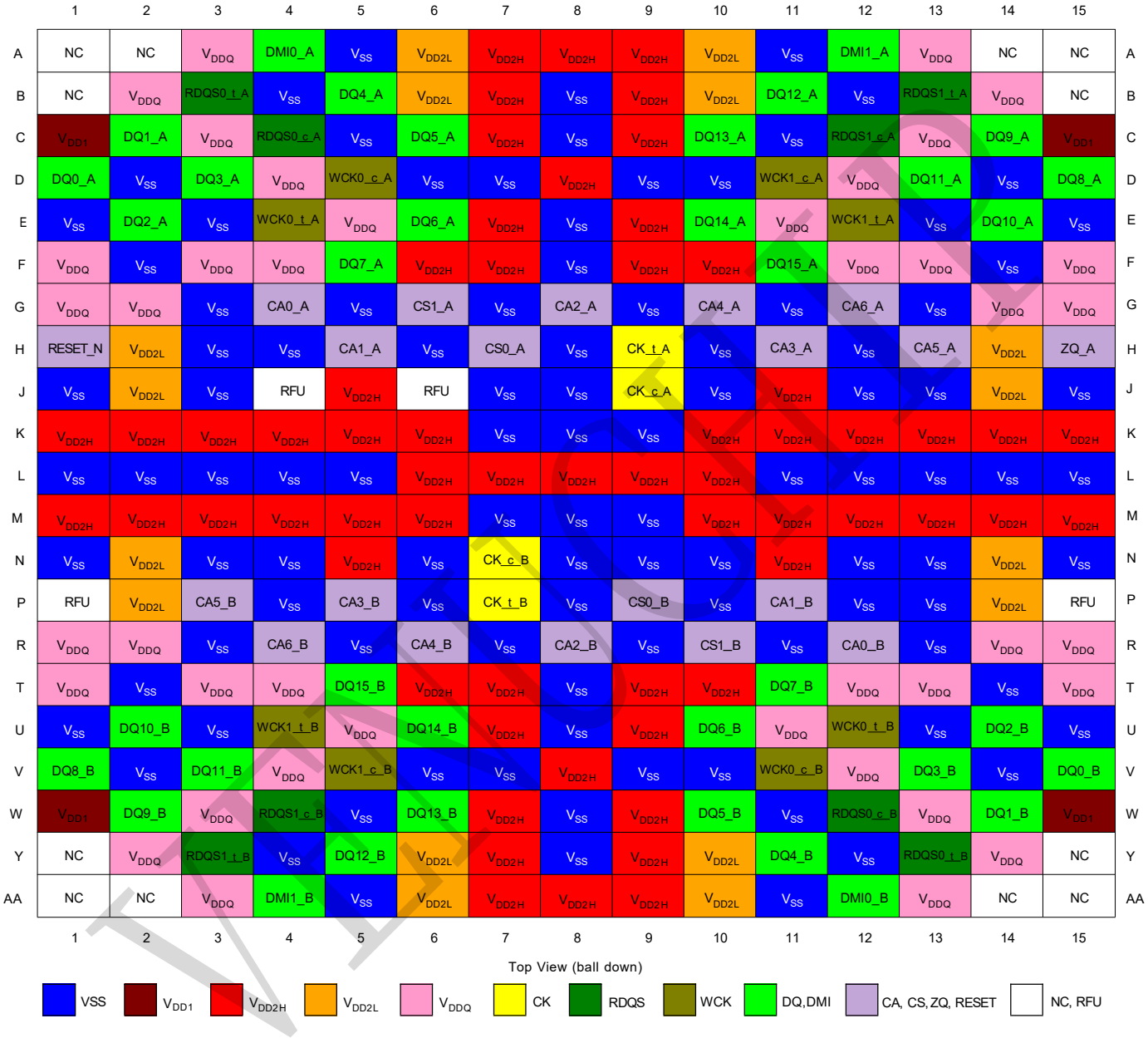
Ball Assignments and Descriptions

315b Dual Channel, 1 Rank, 2 Rank

Table 5: 315-Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:B], CK_c_[A:B]	Input	**Clock:** CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:B], CS1_[A:B]	Input	**Chip select:** CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:B] become NC pins in a single-rank package.
CA[6:0]_[A:B]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:B], WCK[1:0]_c_[A:B]	Input	**Data clock:** WCK_t and WCK_c are differential clock inputs used for write data capture and read data output.
DQ[15:0]_[A:B]	I/O	**Data input/output:** Bidirectional data bus.
RDQS[1:0]_t_[A:B], RDQS[1:0]_c_[A:B]	I/O Output	**Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:B]	I/O	**Data maskinversion:** DMI serves multiple functions such as data mask (DM),data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V_{DDQ} through a 240Ω ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2H}, V_{DD2L}	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
V_{SS}	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**Reset:** When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	**No connect:** Not internally connected.
RFU	–	**Reserved Future Use:** Not internally connected.

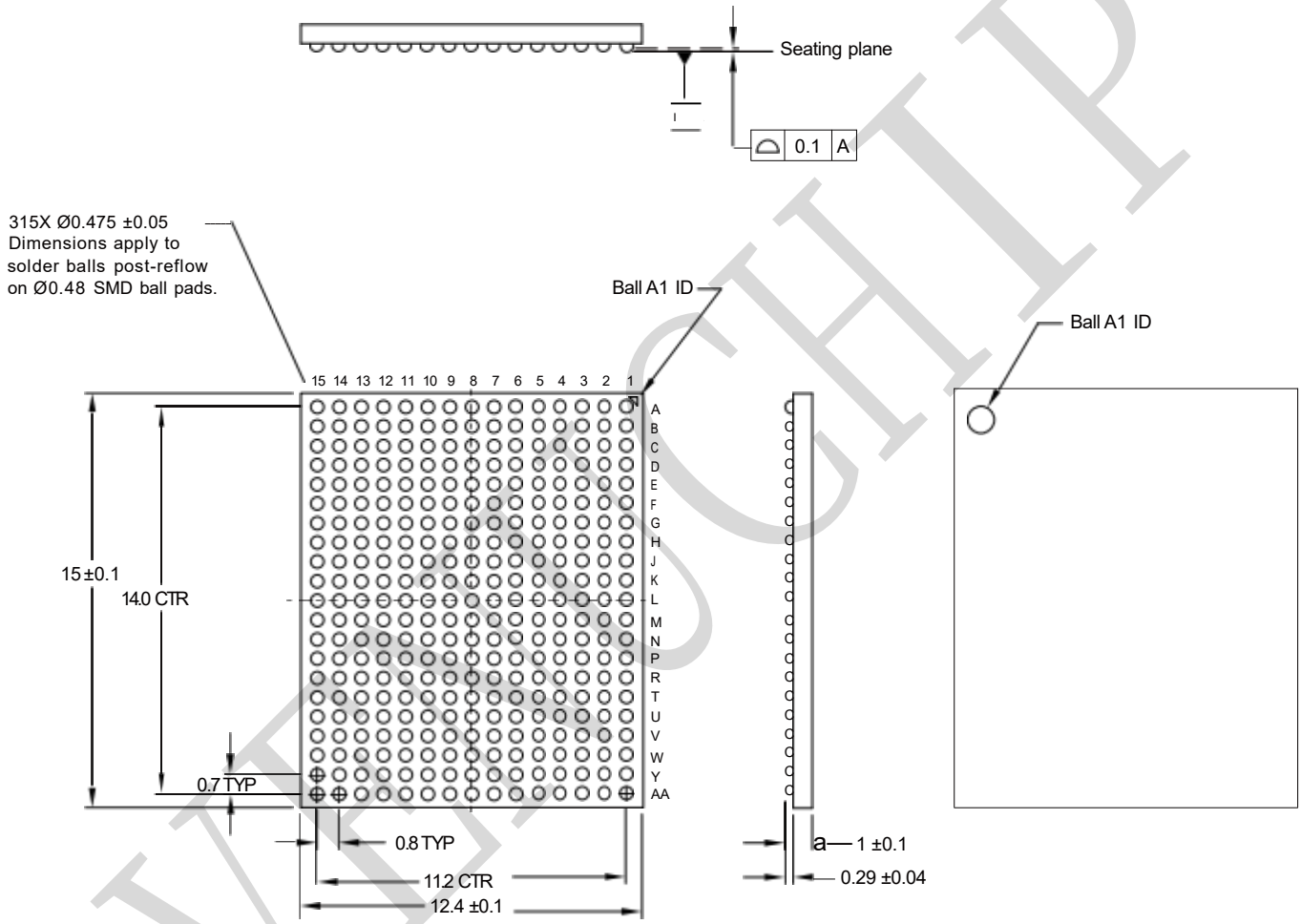
Figure 4：315-Ball Dual-Channel Discrete FBGA



Package Dimensions

315-Ball Package (Package Code: DS)

Figure 5: 315-Ball TFBGA – 12.4mm (TYP) × 15.0mm (TYP) × 1.1mm (MAX) (Package Code: DS)



Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SACQ with CuOSP pads (Sn-4Ag-0.5Cu-3Bi-0.05Ni)

Product-Specific Mode Register Definition

Table 6: Mode Register Contents

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0	**Per pin DFE**	**Pre Emphasis**	**Unified NT ODT behavior mode**	**DMI output behavior mode**	**Optimized refresh mode**	**Enhanced WCK always-on mode**	**Latency mode**	**NT ODT timing mode**
	OP[0] = 1b: Device supports different NT ODT latency for DQ and RDQS							
	OP[1] = 0b: Device supports x16 mode latency							
	OP[2] = 1b: Device supports enhanced WCK always-on mode							
	OP[3] = 1b: Device supports optimized refresh mode							
	OP[4] = 1b: Device supports both DMI behavior mode 1 and 2 and mode selection							
	OP[5] = 1b: The NT ODT behavior follows the unified NT ODT behavior							
	OP[6] = 1b: Device supports Pre Emphasis mode							
	OP[7] = 0b: Device does not support Per pin DFE							
MR1							**ARFM support**	**CS ODT OP support**
	OP[0] = 1b: Device supports CS ODT behavior OP							
	OP[1] = 0b: Device does not support ARFM							
MR3				**BK/BG ORG**				
	OP[4:3] = 00b: BG, 01b: 8B, 10b: 16B Mode supported							
MR5	**Manufacturer ID**							
	1111 1111b: Venuchip							
MR6	**Revision ID1**							
	0000 0111b							
MR8	**I/O width**		**Density**				**Type**	
	OP[7:6] = 00b: x16		OP[5:2] = 0110b: 16Gb				OP[1:0] = 00b: LPDDR5 SDRAM	
MR13						**VRO**		
	OP[2] = 0b: Normal operation (default) 1b: Output the $V_{REF(CA)}$ value on DQ7 and $V_{REF(DQ)}$ value on DQ6							
MR19			**WCK2DQ OSC FM**					
	OP[5] = 1b: WCK2DQ OSC FM supported							
MR21	**WXS**				**ODTD-CSFS**	**WXFS**	**RDCFS**	**WDCFS**
	OP[0] = 1b: WRITE DATA COPY function supported							
	OP[1] = 1b: READ DATA COPY function supported							
	OP[2] = 1b: WRITE X function supported							
	OP[3] = 1b: Device ODTD-CS is supported							
	OP[7] = 1b: Data to be written can be selected with 0 and 1							

Table 6: Mode Register Contents (Continued)

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR22	**RECC**		**WECC**					
	OP[5:4] = 00b: Write link ECC disabled (default) 01b: Write link ECC enabled (See Note 3)							
	OP[7:6] = 00b: Read link ECC disabled (default) 01b: Read link ECC enabled (See Note 3)							
MR24	**DFES**				**Read DCA**			
	OP[3] = 1b: Device supports Read DCA							
	OP[7] = 1b: Device supports DFE							
MR26		**RDQSTFS**						
	OP[6] = 1b: Read/write-based RDQS_t TRAINING function supported							
MR27								**RFM**
	OP[0] = 0b: RFM is not required							
MR43		**SBEC rule**						
	OP[6] = 1b: Simultaneous SBE on each DQ byte and DMI are independently counted							

Notes: 1. The contents of mode registers described here reflect information specific to each die in these packages.
2. Refer to General LPDDR5/LPDDR5X Specification 1 for mode registers not described here.
3. Write link ECC and read link ECC are supported.

I_{DD} Parameters

Refer to I_{DD} Specification Parameters and Test Conditions section in General LPDDR5 Specifications 2 for detailed conditions.

Table 7: I_{DD} Parameters – Single Die

Symbol	Supply	Speed Grade	Unit	Note
		6400 Mb/s		
I_{DD01}	V_{DD1}	3.9	mA	
I_{DD02H}	V_{DD2H}	34.8		
I_{DD02L}	V_{DD2L}	0.3		
I_{DD0Q}	V_{DDQ}	0.8		
I_{DD2P1}	V_{DD1}	1.8	mA	
I_{DD2P2H}	V_{DD2H}	3.0		
I_{DD2P2L}	V_{DD2L}	0.3		
I_{DD2PQ}	V_{DDQ}	0.8		
I_{DD2PS1}	V_{DD1}	1.8	mA	
$I_{DD2PS2H}$	V_{DD2H}	3.0		
$I_{DD2PS2L}$	V_{DD2L}	0.3		
I_{DD2PSQ}	V_{DDQ}	0.8		
I_{DD2N1}	V_{DD1}	1.8	mA	
I_{DD2N2H}	V_{DD2H}	20.4		
I_{DD2N2L}	V_{DD2L}	0.3		
I_{DD2NQ}	V_{DDQ}	0.8		
I_{DD2NS1}	V_{DD1}	1.8	mA	
$I_{DD2NS2H}$	V_{DD2H}	20.4		
$I_{DD2NS2L}$	V_{DD2L}	0.3		
I_{DD2NSQ}	V_{DDQ}	0.8		
I_{DD3P1}	V_{DD1}	1.8	mA	
I_{DD3P2H}	V_{DD2H}	7.8		
I_{DD3P2L}	V_{DD2L}	0.3		
I_{DD3PQ}	V_{DDQ}	0.8		
I_{DD3PS1}	V_{DD1}	1.8	mA	
$I_{DD3PS2H}$	V_{DD2H}	7.8		
$I_{DD3PS2L}$	V_{DD2L}	0.3		
I_{DD3PSQ}	V_{DDQ}	0.8		

Table 7: I_{DD} Parameters – Single Die

Symbol	Supply	Speed Grade	Unit	Note
		6400 Mb/s		
I_{DD3N1}	V_{DD1}	2.2	mA	
I_{DD3N2H}	V_{DD2H}	26.0		
I_{DD3N2L}	V_{DD2L}	0.3		
I_{DD3NQ}	V_{DDQ}	0.8		
I_{DD3NS1}	V_{DD1}	2.2	mA	
$I_{DD3NS2H}$	V_{DD2H}	26.0		
$I_{DD3NS2L}$	V_{DD2L}	0.3		
I_{DD3NSQ}	V_{DDQ}	0.8		
I_{DD4R1}	V_{DD1}	13.0	mA	3, 4
I_{DD4R2H}	V_{DD2H}	426.0		
I_{DD4R2L}	V_{DD2L}	0.3		
I_{DD4RQ}	V_{DDQ}	128.0		
I_{DD4W1}	V_{DD1}	12.0	mA	3
I_{DD4W2H}	V_{DD2H}	318.0		
I_{DD4W2L}	V_{DD2L}	0.3		
I_{DD4WQ}	V_{DDQ}	0.8		
I_{DD51}	V_{DD1}	28.0	mA	
I_{DD52H}	V_{DD2H}	198.0		
I_{DD52L}	V_{DD2L}	0.3		
I_{DD5Q}	V_{DDQ}	0.8		
I_{DD5AB1}	V_{DD1}	3.9	mA	
$I_{DD5AB2H}$	V_{DD2H}	33.0		
$I_{DD5AB2L}$	V_{DD2L}	0.3		
I_{DD5ABQ}	V_{DDQ}	0.8		
I_{DD5PB1}	V_{DD1}	3.9	mA	
$I_{DD5PB2H}$	V_{DD2H}	33.0		
$I_{DD5PB2L}$	V_{DD2L}	0.3		
I_{DD5PBQ}	V_{DDQ}	0.8		

Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. BG mode. DVFSC and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF, R_{ON} = 40 ohm, T_C = 25。C.
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V; T_C = –25。C to +85。C
6. Notes 1, 2, and 5 apply to entire table.

Table 8: Full-Array Power-Down Self Refresh Current – Single Die

Temperature	Symbol	Supply	Value	Unit
85。C	I_{DD61}	V_{DD1}	4.0	
	I_{DD62H}	V_{DD2H}	16.0	
	I_{DD62L}	V_{DD2L}	0.3	
	I_{DD6Q}	V_{DDQ}	0.8	

Notes: 1. I_{DD6}85。C is the maximum I_{DD} guaranteed value considering the worst-case conditions of process, temperature, and voltage.
2. DVFSC and DVFSQ disabled.
3. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V; T_C = –25。C to +85。C