4Gb DDR3L SDRAM

VN3R256M16M-16H
VN3R256M16M-18H
VN3R256M16MI-18H

Contents

1 Overview

This chapter gives an overview of the 4Gbit DDR3L SDRAM component product and describes its main characteristics.

1.1 Features

The 4Gbit DDR3L SDRAM offers the following key features:

- VDD,=VDDQ=1.35V(1.283V-1.45V)
  - Backward compatible to VDD=VDDQ=(1.5 V ±0.075V)

-Supports DDR3L devices to be backward compatible in 1.5V applications

- Data rate :1600Mbps/1866Mbps/2133Mbps
- Differential bidirectional data strobe
- 8*n*-bit prefetcharchitecture
- Differential clock inputs (CK, CKB)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS (READ) latency (CL)

• Programmable posted CAS additive latency (AL)
• Programmable CAS (WRITE) latency (CWL)
• Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
• Selectable BC4 or BL8 on-the-fly (OTF)
• Self-refresh mode
• TC of 0°C to + 95°C
– 64ms, 8192-cycle refresh at 0°C to +85°C
– 32ms at +85°C to +95°C
• Self refresh temperature (SRT)
• Automatic self refresh (ASR)
• Write leveling
• Multi-purpose register
• Output driver calibration

Options
• Configuration
– 512 Meg x 8
– 256 Meg x 16

• FBGA package (Pb-free) – x8 – 78-ball (10.6mm x 7.5mm)

• FBGA package (Pb-free) – x16 – 96-ball (13.5mm x 7.5mm)

• Timing – cycle time
– 938ps @ CL = 14 (DDR3-2133)
– 1.07ns @ CL = 13 (DDR3-1866)
– 1.25ns @ CL = 11 (DDR3-1600)

• Operating temperature
– Commercial, (0°C ≤TC ≤ +95°C)
– Industrial, (-40°C ≤TC ≤ +95°C)

1.2 Product List

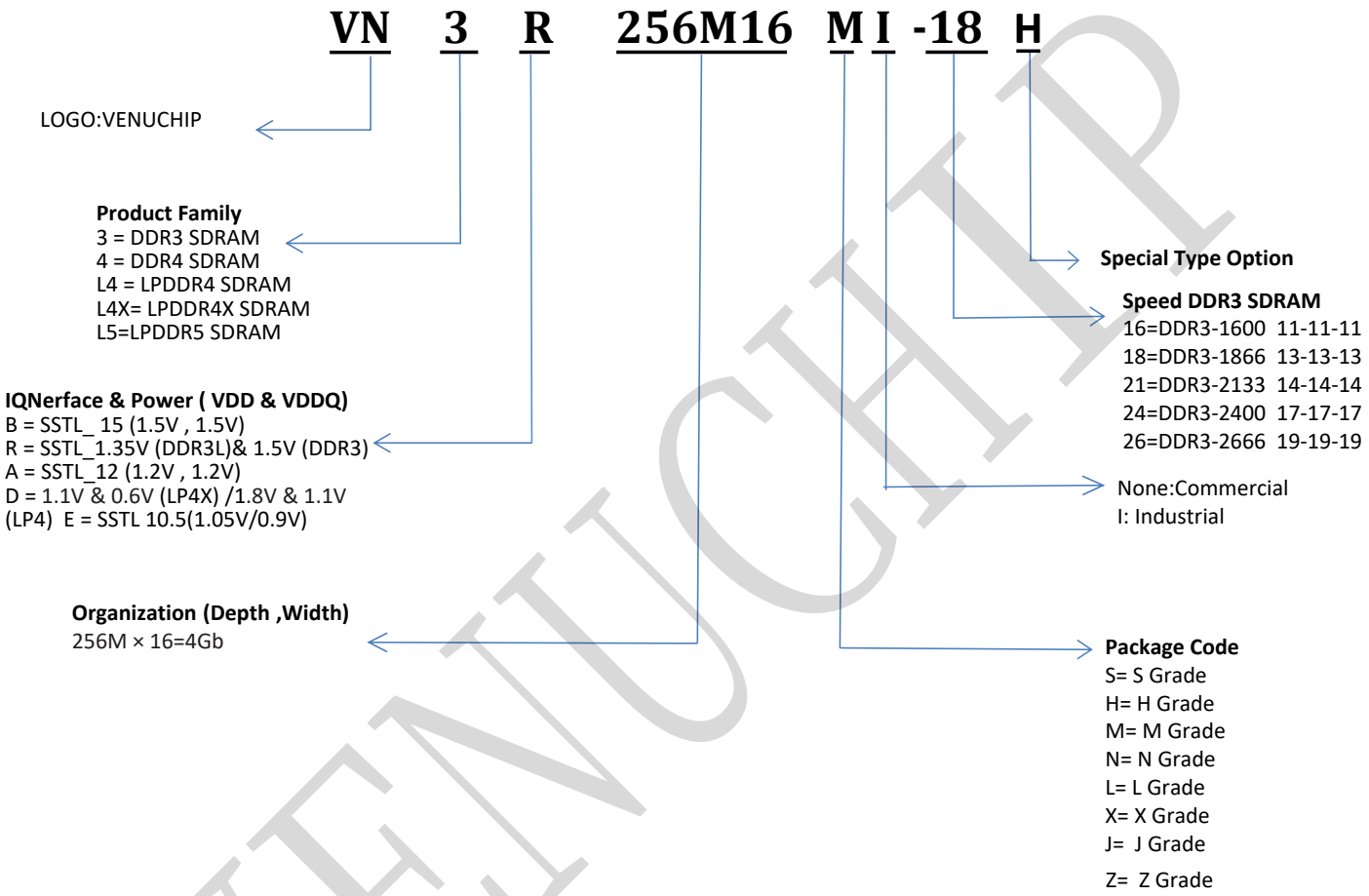
Table 1 shows all possible products within the 4Gbit DDR3L SDRAM component generation. Availability depends on application needs. For Venuchip part number nomenclature see **Chapter 6**.

Table 1 - Ordering Information for4Gbit DDR3L Components

Venuchip Part Number	Max. Clock frequency	Org	CAS-RCD-RP latencies	Speed Sort Name	Package
VN3R256M16M-16H	800 MHz	× **16**	11-11-11	DDR3L–1600M	96 FBGA
VN3R256M16M-18H	933 MHz	× **16**	13-13-13	DDR3L–1866M	96 FBGA
VN3R256M16MI-18H	933 MHz	× **16**	13-13-13	DDR3L–1866M	96 FBGA

Part Numbering Information

Venuchip Component Part Numbering Guide



1.3 DDR3 SDRAM Addressing

Table 2 - 4Gbit DDR3 SDRAM Addressing

Configuration	**512Mb × 8**	**256Mb × 16**	**Note**
Internal Organization	8 banks × 64M words × 8bits	8 banks × 32M words × 16bits	
Refresh count	8K	8K	
Bank Address	8(BA[2:0])	8(BA[2:0])	
Row Address	64K (A[15:0])	32K (A[14:0])	
Column Address	1K(A[9:0])	1K(A[9:0])	
Page Size	1KB	2KB	

1.4 Package Ball out

Figure 1 show the ball outs for DDR3 SDRAM components. See **Chapter 5** for package outlines.

1.4.1 Ball out for 512 Mb ×8 Components

Figure 1 - Ball out for 512 Mb ×8 Components (PG-TFBGA-78)

1	2	3	4	5	6	7	8	9
VSS	VDD	NC		A		NU/TDQS#	VSS	VDD
VSS	VSSQ	DQ0		B		DM/TDQS	VSSQ	VDDQ
VDDQ	DQ2	DQS		C		DQ1	DQ3	VSSQ
VSSQ	DQ6	DQS#		D		VDD	VSS	VSSQ
VREFDQ	VDDQ	DQ4		E		DQ7	DQ5	VDDQ
NC	VSS	RAS#		F		CK	VSS	NC
ODT	VDD	CAS#		G		CK#	VDD	CKE
NC	CS#	WE#		H		A10/AP	ZQ	NC
VSS	BA0	BA2		J		A15	VREFCA	VSS
VDD	A3	A0		K		A12/BC#	BA1	VDD
VSS	A5	A2		L		A1	A4	VSS
VDD	A7	A9		M		A11	A6	VDD
VSS	RESET#	A13		N		A14	A8	VSS

1.4.2 Ball out for 256 Mb ×16 Components

Figure 2 - Ball out for 256 Mb ×16 Components (PG-TFBGA-96)

1	2	3	4	5	6	7	8	9
VDDQ	DQU5	DQU7		A		DQU4	VDDQ	VSS
VSSQ	VDD	VSS		B		DQSU#	DQU6	VSSQ
VDDQ	DQU3	DQU1		C		DQSU	DQU2	VDDQ
VSSQ	VDDQ	DMU		D		DQU0	VSSQ	VDD
VSS	VSSQ	DQL0		E		DML	VSSQ	VDDQ
VDDQ	DQL2	DQSL		F		DQL1	DQL3	VSSQ
VSSQ	DQL6	DQSL#		G		VDD	VSS	VSSQ
VREFDQ	VDDQ	DQL4		H		DQL7	DQL5	VDDQ
NC	VSS	RAS#		J		CK	VSS	NC
ODT	VDD	CAS#		K		CK#	VDD	CKE
NC	CS#	WE#		L		A10/AP	ZQ	NC
VSS	BA0	BA2		M		NC	VREFCA	VSS
VDD	A3	A0		N		A12/BC#	BA1	VDD
VSS	A5	A2		P		A1	A4	VSS
VDD	A7	A9		R		A11	A6	VDD
VSS	RESET#	A13		T		A14	A8	VSS

1.5 Input / Output Signal Functional Description

Table 3 - Input / Output Signal Functional Description

Symbol	Type	Function
CK, /CK	Input	**Clock:** CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK.
CKE	Input	**Clock Enable:** CKE High activates, and CKE Low deactivates internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (active row in any bank). CKE is asynchronous for Self-Refresh exit. After V_{REFCA} and V_{REFDQ} have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained High throughout read and write accesses. Input buffers, excluding CK, /CK, ODT, CKE and /RESET are disabled during Power-down. Input buffers, excluding CKE and RESET are disabled during self refresh.
/CS	Input	**Chip Select:** All commands are masked when /CS is registered High. /CS provides for external Rank selection on systems with multiple ranks. /CS is considered part of the command code.
/RAS, /CAS, /WE	Input	**Command Inputs:** /RAS, /CAS and /WE (along with /CS) define the command being entered.
		On-Die Termination: ODT (registered High) enables termination resistance DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, /DQS and DM signal for×8 configurations. The ODT signal will be ignored if the Mode Register MR1 is programmed to disable ODT and during Self Refresh.
DM	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a Write access. DM is sampled on both edges of DQS.
BA0 - BA2	Input	**Bank Address Inputs:** Define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a mode register set cycle.
A0 – A15	Input	**Address Inputs:** Provides the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12 | /BC have additional functions, see below). The address inputs also provide the op-code during Mode Register Set commands.
A10 | AP	Input	**Auto-Precharge:**A10 | AP is sampled during Read/Write commands to determine whether Auto-Precharge should be performed to the accessed bank after the Read/Write operation. (High: Auto-Precharge, Low: no Auto-Precharge).A10 | AP is sampled during Precharge command to determine whether the Precharge applies to one bank (A10 Low) or all banks (A10 High). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 | /BC	Input	**Burst Chop:** A12 | /BC is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (High: no burst chop, Low: burst chopped). See **"Command Truth Table" on Page 11** for details.
DQ	Input/ Output	**Data Input/Output:** Bi-directional data bus.
DQS /DQS	Input/ Output	**Data Strobe:** output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobes DQS are paired with differential signals /DQS, to provide differential pair signaling to the system during both read and write. DDR3

Symbol	Type	Function
/RESET	CMOS Input	**Active Low Asynchronous Reset:** Reset is active when /RESET is Low, and inactive when /RESET is High. /RESET must be High during normal operation. /RESET is a CMOS rail to rail signal with DC High and Low are 80% and 20% of V_{DD}, /RESET active is destructive to data contents.
NC	—	**No Connect:** no internal electrical connection is present
V_{DDQ}	Supply	**DQ Power Supply:** 1.283V to 1.45V or 1.5 V ±0.075V
V_{SSQ}	Supply	**DQ Ground**
V_{DD}	Supply	**Power Supply:** 1.283V to 1.45V or 1.5 V ±0.075V
V_{SS}	Supply	**Ground**
V_{REFDQ}	Supply	**Reference Voltage for DQ**
V_{REFCA}	Supply	**Reference Voltage for Command and Address inputs**
ZQ	Supply	Reference ball for ZQ calibration

Note: Input only pins (BA0-BA2, A0-A15, /RAS, /CAS, /WE, /CS, CKE, ODT, and /RESET) do not supply termination.

2 Functional Description

2.1 Truth Tables

The truth tables list the input signal values at a given clock edge which represent a command or state transition expected to be executed by the DDR3 SDRAM. **Table 4** lists all valid commands to the DDR3 SDRAM. For a detailed description of the various power mode entries and exits please refer to **Table 5**. In addition, the DM functionality is described in **Table 6**.

Table 4 - Command Truth Table

Function	Abbr.	CKE		/CS	/RAS	/CAS	/WE	BA2 - BA0	A13-A15	A12|/BC	A10|AP	A11, A9-A0	Note
		Prev. Cycle	Curr. Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				1)2)3)4)5)
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	1)2)3)4)5)
Self-Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	1)2)3)4)5)6)7)8)
Self-Refresh Exit	SRX	L	H	H	V	V	V	V	V	V	V	V	1)2)3)4)5)6)7)8)9)
				L	H	H	H						
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	1)2)3)4)5)
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	1)2)3)4)5)
Active	ACT	H	H	L	L	H	H	BA	RA (Row Address)				1)2)3)4)5)
Write (BL8MRS or BC4MRS)	WR	H	H	L	H	L	L	BA	V	V	L	CA	1)2)3)4)5)10)
Write (BC4OTF)	WRS4	H	H	L	H	L	L	BA	V	L	L	CA	1)2)3)4)5)10)
Write (BL8OTF)	WRS8	H	H	L	H	L	L	BA	V	H	L	CA	1)2)3)4)5)10)
Write w/AP (BL8MRS or BC4MRS)	WRA	H	H	L	H	L	L	BA	v	V	H	CA	1)2)3)4)5)10)
Write w/AP (BC4OTF)	WRAS4	H	H	L	H	L	L	BA	V	L	H	CA	1)2)3)4)5)10)
Write w/AP (BL8OTF)	WRAS8	H	H	L	H	L	L	BA	V	H	H	CA	1)2)3)4)5)10)
Read (BL8MRS or BC4MRS)	RD	H	H	L	H	L	H	BA	V	V	L	CA	1)2)3)4)5)10)
Read (BC4OTF)	RDS4	H	H	L	H	L	H	BA	V	L	L	CA	1)2)3)4)5)10)
Read (BL8OTF)	RDS8	H	H	L	H	L	H	BA	V	H	L	CA	1)2)3)4)5)10)
Read w/AP (BL8MRS or BC4MRS)	RDA	H	H	L	H	L	H	BA	V	V	H	CA	1)2)3)4)5)10)
Read w/AP (BC4OTF)	RDAS4	H	H	L	H	L	H	BA	V	L	H	CA	1)2)3)4)5)10)
Read w/AP (BL8OTF)	RDAS8	H	H	L	H	L	H	BA	V	H	H	CA	1)2)3)4)5)10)
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	1)2)3)4)5)11)

Function	Abbr.	CKE		CS	RAS	CAS	WE	BA2 - BA0	A13 A14 A15	A12| /BC	A10/ AP	A11, A9-A0	Note
		Prev. Cycle	Curr. Cycle										
Device Deselect	DES	H	H	H	X	X	X	X	X	X	X	X	1)2)3)4)5)12)
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	1)2)3)4)5)8)13)
				H	V	V	V						
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	1)2)3)4)5)8)13)
				H	V	V	V						
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	1)2)3)4)5)
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	1)2)3)4)5)

1) BA = Bank Address, RA = Row Address, CA = Column Address, BC = Burst Chop, AP = Auto Precharge, X = Don't care, V = valid
2) All DDR3 SDRAM commands are defined by states of /CS, /RAS, /CAS, /WE and CKE at the rising edge of the clock. The higher order address bits of BA, RA and CA are device density and IO configuration (×4, ×8, ×16) dependent.
3) /RESET is a low active signal which will be used only for asynchronous reset. It must be maintained High during any function.
4) Bank addresses (BA) determine which bank is to be operated upon. For MRS, BA selects a Mode Register.
5) V means H or L (but a defined logic level) and X means either "defined or undefined (like floating) logic level".
6) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh
7) V_{REF} (both V_{REFCA} and V_{REFDQ}) must be maintained during Self Refresh operation.
8) Refer to **"Clock Enable (CKE) Truth Table for Synchronous Transitions" on Page 13** for more detail with CKE transition.
9) Self refresh exit is asynchronous.
10) Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.
11) The No Operation (NOP) command should be used in cases when the DDR3 SDRAM is in an idle or a wait state. The purpose of the NOP command is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A NOP command will not terminate a previous operation that is still executing, such as a read or write burst.
12) The Deselect command (DES) performs the same function as a No Operation command.
13) The Power Down Mode does not perform any refresh operation.

Table 5 - Clock Enable (CKE) Truth Table for Synchronous Transitions

Current State [1]	CKE(N-1)[2]	CKE(N)[2]	Command (N)[3] /RAS, /CAS, /WE, /CS	Action (N)[3]	Note
	Previous Cycle	Current Cycle			
Power Down	L	L	X	Maintain Power Down	4)5)6)7)8)9)
	L	H	DES or NOP	Power Down Exit	4)5)6)7)8)10)
Self Refresh	L	L	X	Maintain Self Refresh	4)5)6)7)9)11)
	L	H	DES or NOP	Self Refresh Exit	4)5)6)7)11)12)13)
Bank(s) Active	H	L	DES or NOP	Active Power Down Entry	4)5)6)7)8)10)14)
Reading	H	L	DES or NOP	Power Down Entry	4)5)6)7)8)10)14)15)
Writing	H	L	DES or NOP	Power Down Entry	4)5)6)7)8)10)14)15)
Precharging	H	L	DES or NOP	Power Down Entry	4)5)6)7)8)10)14)15)
Refreshing	H	L	DES or NOP	Precharge Power Down Entry	4)5)6)7)10)
All Banks Idle	H	L	DES or NOP	Precharge Power Down Entry	4)5)6)7)10)8)14)16)
	H	L	REF	Self Refresh Entry	4)5)6)7)14)16)17)
Any other state	Refer to **"Command Truth Table" on Page 11** for more detail with all command signals				4)5)6)7)18)

1) Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.
2) CKE(N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
3) COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N),ODT is not included here.
4) All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
6) CKE must be registered with the same value on $t_{CKE.MIN}$ consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the $t_{CKE.MIN}$ clocks of registeration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + $t_{CKE.MIN}$ + t_{IH}.
7) DES and NOP are defined in **"Command Truth Table" on Page 11**.
8) The Power Down does not perform any refresh operations
9) X means Don't care (including floating around V_{REFCA}) in Self Refresh and Power Down. It also applies to address pins.
10) Valid commands for Power Down Entry and Exit are NOP and DES only
11) V_{REF} (both V_{REFCA} and V_{REFDQ}) must be maintained during Self Refresh operation.
12) On Self Refresh Exit DES or NOP commands must be issued on every clock edge occurring during the t_{XS} period. Read, or ODT commands may be issued only after t_{XSDLL} is satisfied.
13) Valid commands for Self Refresh Exit are NOP and DES only.
14) Self Refresh can not be entered while Read or Write operations are in progress.
15) If all banks are closed at the conclusion of a read, write or precharge command then Precharge Power-down is entered, otherwise Active Power-down is entered.
16) 'Idle state' is defined as all banks are closed (t_{RP}, t_{DAL}, etc. satisfied), no data bursts are in progress, CKE is High, and all timings from previous operations are satisfied (t_{MRD}, t_{MOD}, t_{RFC}, $t_{ZQ.INIT}$, $t_{ZQ.OPER}$, t_{ZQCS}, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (t_{XS}, t_{XP}, t_{XPDLL}, etc.).
17) Self Refresh mode can only be entered from the All Banks Idle state.
18) Must be a legal command as defined in **"Command Truth Table" on Page 11**.

Table 6 - Data Mask (DM) Truth Table

Name (Function)	DM	DQs
Write Enable	L	Valid
Write Inhibit	H	X

2.2 Mode Register 0 (MR0)

The mode register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR (write recovery time for auto-precharge) and DLL control for precharge Power-Down, which includes various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting Low on /CS, /RAS, /CAS, /WE, BA0, BA1, and BA2, while controlling the states of address pins according to **Table 7**.

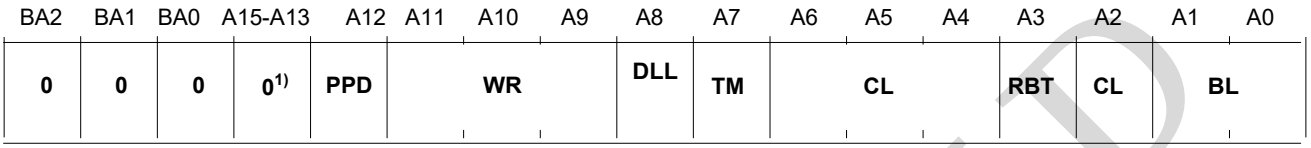


Table 7 - MR0 Mode register Definition (BA[2:0]=000B)

Field	Bits[1)]	Description
BL	A[1:0]	**Burst Length (BL) and Control Method** Number of sequential bits per DQ related to one Read/Write command. 00_B **BL8MRS** mode with fixed burst length of 8. A12 | /BC at Read or Write command time is Don't care at read or write command time. 01_B **BLOTF** on-the-fly (OTF) enabled using A12 | /BC at Read or Write command time. When A12 | /BC is High during Read or Write command time a burst length of 8 is selected (BL8OTF mode). When A12 | /BC is Low, a burst chop of 4 is selected (BC4OTF mode). Auto-Precharge can be enabled or disabled. 10_B **BC4MRS** mode with fixed burst chop of 4 with $t_{CCD} = 4 \times n_{CK}$. A12 | /BC is Don't care at Read or Write command time. 11_B **TBD** Reserved
RBT	A3	**Read Burst Type** 0_B Nibble Sequential 1_B Interleaved
CL	A[6:4,2]	**CAS Latency (CL)** CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. *Note: For more information on the supported CL and AL settings based on the operating clock frequency, refer to **"Speed Bins" on Page 33**.* *Note: All other bit combinations are reserved.* 0000_B RESERVED 0010_B 5 0100_B 6 0110_B 7 1000_B 8 1010_B 9 1100_B 10 1110_B

Field	Bits[1)]	Description
TM	A7	**Test Mode** The normal operating mode is selected by MR0(bit A7 = 0) and all other bits set to the desired values shown in this table. Programming bit A7 to a 1 places the DDR3 SDRAM into a test mode that is only used by the SDRAM manufacturer and should NOT be used. No operations or functionality is guaranteed if A7 = 1. 0_B Normal Mode 1_B Vendor specific test mode
DLLres	A8	**DLL Reset** The internal DLL Reset bit is self-clearing, meaning it returns back to the value of 0 after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time the DLL reset function is used, t_{DLLK} must be met before any functions that require the DLL can be used (i.e. Read commands or synchronous ODT operations). 0_B No DLL Reset 1_B DLL Reset triggered
WR	A[11:9]	**Write Recovery for Auto-Precharge** Number of clock cycles for write recovery during Auto-Precharge. WR_{MIN} in clock cycles is calculated by dividing $t_{WR.MIN}$ (in ns) by the actual $t_{CK.AVG}$ (in ns) and rounding up to the next integer: WR.MIN [n_{CK}] = Roundup($t_{WR.MIN}$[ns] / $t_{CK.AVG}$[ns]). The WR value in the mode register must be programmed to be equal or larger than WR.MIN. The resulting WR value is also used with t_{RP} to determine t_{DAL}. Since WR of 9 and 11 is not implemented in DDR3 and the above formula results in these values, higher values have to be programmed. 000_B Reserved 001_B 5 010_B 6 011_B 7 100_B 8 101_B 10 110_B 12 111_B Reserved
PPD	A12	**Precharge Power-Down DLL Control** Active Power-Down will always be with DLL-on. Bit A12 will have no effect in this case. For Precharge Power-Down, bit A12 in MR0 is used to select the DLL usage as shown below. 0_B **Slow Exit.** DLL is frozen during precharge Power-down.Read and synchronous ODT commands are only allowed after t_{XPDLL}. 1_B **Fast Exit.** DLL remains on during precharge Power-down.Any command can be applied after t_{XP}, provided that other timing parameters are satisfied.

1) A13, A14 and A15 - even if not available on a specific device - must be programmed to 0_B.

2.3 Mode Register 1 (MR1)

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, $R_{TT_}$Nom impedance, additive latency (AL), Write leveling enable and Qoff (output disable). The Mode Register MR1 is written by asserting Low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, High on BA0 and Low on BA1and BA2, while controlling the states of address pins according to **Table 8.**

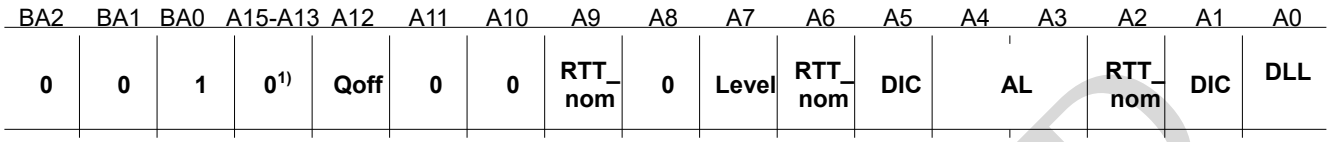


Table 8 - MR1 Mode Register Definition (BA[2:0]=001B)

Field	Bits[1)]	Description
DLLdis	A0	**DLL Disable** The DLL must be enabled for normal operation. DLL enable is required during power up initialization, after reset and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1(A0 = 0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled and reset upon exit of Self-Refresh operation. Any time the DLL is enabled, a DLL reset must be issued afterwards. Any time the DLL is reset, t_{DLLK} clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the t_{DQSCK}, t_{AON}, t_{AOF} or t_{ADC} parameters. During t_{DLLK}, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation. 0_B DLL is enabled 1_B DLL is disabled
DIC	A[5, 1]	**Output Driver Impedance Control** *Note: All other bit combinations are reserved.* 00: RZQ/6 01_B Nominal Drive Strength RON34 = RQZ/7 (nominal 34.3 Ω, with nominal RZQ = 240 Ω)
R_{TT_NOM}	A[9, 6, 2]	**Nominal Termination Resistance of ODT** **Notes** *1. If R_{TT_NOM} is used during Writes, only the values R_{ZQ}/2, R_{ZQ}/4 and R_{ZQ}/6 are allowed.* *2. In Write leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 1, all $R_{TT_}$Nom settings are allowed; in Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 0, only R_{TT_NOM} settings of R_{ZQ}/2, R_{ZQ}/4 and R_{ZQ}/6 are allowed.* *3. All other bit combinations are reserved.* 000_B ODT disabled, R_{TT_NOM} = off, Dynamic ODT mode disabled 001_B RTT60 = RZQ / 4 (nominal 60 Ω with nominal RZQ = 240 Ω) 010_B RTT120 = RZQ / 2 (nominal 120 Ω with nominal RZQ = 240 Ω 011_B RTT40 = RZQ / 6 (nominal 40 Ω with nominal RZQ = 240 Ω) 100_B RTT20 = RZQ / 12 (nominal 20 Ω with nominal RZQ = 240 Ω) 101_B RTT30 = RZQ / 8 (nominal 30 Ω with nominal RZQ = 240 Ω)

Field	Bits[1)]	Description
AL	A[4, 3]	**Additive Latency (AL)** Any read or write command is held for the time of Additive Latency (AL) before it is issued as internal read or write command. **Notes** *1. AL has a value of CL - 1 or CL - 2 as per the CL value programmed in the MR0 register.* 00_B AL = 0 (AL disabled) 01_B AL = CL - 1 10_B AL = CL - 2 $_B$ Reserved
Write Leveling enable	A7	**Write Leveling Mode** 0_B **Write Leveling Mode** Disabled, Normal operation mode 1_B **Write Leveling Mode** Enabled
TDQS enable	A11	0: Disabled 1: Enabled
Qoff	A12	**Output Disable** Under normal operation, the SDRAM outputs are enabled during read operation and write leveling for driving data (Qoff bit in the MR1 is set to 0_B). When the Qoff bit is set to 1_B, the SDRAM outputs (DQ, DQS, /DQS) will be disabled - also during write leveling. Disabling the SDRAM outputs allows users to run write leveling on multiple ranks and to measure I_{DD} currents during Read operations, without including the output. o_B Output buffer enabled 1_B Output buffer disabled

1) A13, A14, A15 - even if not available on a specific device - must be programmed to 0_B.

2.4 Mode Register 2 (MR2)

The Mode Register MR2 stores the data for controlling refresh related features, R_{TT_WR} impedance, and CAS write latency. The Mode Register MR2 is written by asserting Low on CS, RAS, CAS, WE, High on BA1 and Low on BA0 and BA2, while controlling the states of address signals according to Table 9.

BA2	BA1	BA0	A15-A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	**1**	**0**	**0[1)]**	**0**	**0**	**Rtt_WR**		**0**	**SRT**	**ASR**	**CWL**			**PASR**		

Table 9 - MR2 Mode Register Definition (BA[2:0]=010_B)

Field	Bits[1)]	Description
PASR	A[2:0]	**Partial Array Self Refresh (PASR)** If PASR (Partial Array Self Refresh) is enabled, data located in areas of the array beyond the specified self refresh location may get lost if self refresh is entered. During non-self-refresh operation, data integrity will be maintained if t_{REFI} conditions are met. 000_B Full array (Banks 000_B - 111_B) 001_B Half Array(Banks 000_B - 011_B) 010_B Quarter Array(Banks 000_B - 001_B) 011_B 1/8th array (Banks 000_B) 100_B 3/4 array(Banks 010_B - 111_B) 101_B Half array(Banks 100_B - 111_B) 110_B Quarter array(Banks 110_B - 111_B) 111_B 1/8th array(Banks 111_B)
CWL	A[5:3]	**CAS Write Latency (CWL)** Number of clock cycles from internal write command to first write data in. *Note: All other bit combinations are reserved.* 000_B 5 (3.3 ns ≥ $t_{CK.AVG}$ ≥ 2.5 ns) 001_B 6 (2.5 ns > $t_{CK.AVG}$ ≥ 1.875 ns) 010_B 7 (1.875 ns > $t_{CK.AVG}$ ≥ 1.5 ns) 011_B 8 (1.5 ns > $t_{CK.AVG}$ ≥ 1.25 ns) *Note: Besides CWL limitations on $t_{CK.AVG}$, there are also $t_{AA.MIN/MAX}$ restrictions that need to be observed. For details, please refer to **Chapter 4.1**, **Speed Bins**.*
RFU	A6	**0: Manual SR reference (SRT)** **1: ASR enable (Optional)**.

Field	Bits[1)]	Description
SRT	A7	**Self-Refresh Temperature Range (SRT)** The SRT bit must be programmed to indicate T_{OPER} during subsequent self refresh operation. 0_B Normal operating temperature range 1_B Extended operating temperature range
R_{TT_WR}	A[10:9]	**Dynamic ODT mode and R_{TT_WR} Pre-selection** **Notes** *1. All other bit combinations are reserved.* *2. The R_{TT_WR} value can be applied during writes even when R_{TT_NOM} is disabled. During write leveling, Dynamic ODT is not available.* 00_B Dynamic ODT mode disabled 01_B Dynamic ODT mode enabled with R_{TT_WR} = RZQ/4 = 60 Ω 10_B Dynamic ODT mode enabled with R_{TT_WR} = RZQ/2 = 120Ω

1) A13, A14, A15 - even if not available on a specific device - must be programmed to 0_B.

2.5 Mode Register 3 (MR3)

The Mode Register MR3 controls Multi purpose registers and optional On-die thermal sensor (ODTS) feature. The Mode Register MR3 is written by asserting Low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, High on BA1 and BA0, and Low on BA2 while controlling the states of address signals according to **Table 10**

BA2	BA1	BA0	A15-A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	**1**	**1**	**0[1)]**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**MPR**	**MPR loc**	

Table 10 - MR3 Mode Register Definition (BA[2:0]=011_B)

Field	Bits[1)]	Description
MPR loc	A[1:0]	**Multi Purpose Register Location** 00_B Pre-defined data pattern for read synchronization 01_B RFU 10_B RFU 11_B ODTS On-Die Thermal sensor readout (optional)
MPR	A2	**Multi Purpose Register Enable** *Note: When MPR is disabled, MR3 A[1:0] will be ignored.* 0_B MPR disabled, normal memory operation 1_B Dataflow from the Multi Purpose register MPR

1) A13, A14 and A15 - even if not available on a specific device - must be programmed to 0_B.

2.6 Burst Order

Accesses within a given burst may be interleaved or nibble sequential depending on the programmed bit A3 in the mode register MR0.

Regarding read commands, the lower 3 column address bits CA[2:0] at read command time determine the start address for the read burst.

Regarding write commands, the burst order is always fixed. For writes with a burst length of 8, the inputs on the lower 3 column address bits CA[2:0] are ignored during the write command. For writes with a burst being chopped to 4, the input on column address 2 (CA[2]) determines if the lower or upper four burst bits are selected. In this case, the inputs on the lower 2 column address bits CA[1:0] are ignored during the write command.The following table shows burst order versus burst start address for reads and writes of bursts of 8 as well as of bursts of 4 operation (burst chop).

Table 11 - Bit Order during Burst

Burst Length	READ/ WRITE	Starting Column Address	Burst Type = Sequential (Decimal)	Burst Type = Interleaved (Decimal)	Notes
4 (chop)	READ	0 0 0	0, 1, 2, 3, Z, Z, Z, Z	0, 1, 2, 3, Z, Z, Z, Z	1, 2
		0 0 1	1, 2, 3, 0, Z, Z, Z, Z	1, 0, 3, 2, Z, Z, Z, Z	1, 2
		0 1 0	2, 3, 0, 1, Z, Z, Z, Z	2, 3, 0, 1, Z, Z, Z, Z	1, 2
		0 1 1	3, 0, 1, 2, Z, Z, Z, Z	3, 2, 1, 0, Z, Z, Z, Z	1, 2
		1 0 0	4, 5, 6, 7, Z, Z, Z, Z	4, 5, 6, 7, Z, Z, Z, Z	1, 2
		1 0 1	5, 6, 7, 4, Z, Z, Z, Z	5, 4, 7, 6, Z, Z, Z, Z	1, 2
		1 1 0	6, 7, 4, 5, Z, Z, Z, Z	6, 7, 4, 5, Z, Z, Z, Z	1, 2
		1 1 1	7, 4, 5, 6, Z, Z, Z, Z	7, 6, 5, 4, Z, Z, Z, Z	1, 2
	WRITE	0 V V	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X	1, 3, 4
		1 V V	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X	1, 3, 4
8 (fixed)	READ	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	1
		0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6	1
		0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5	1
		0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4	1
		1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	1
		1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2	1
		1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1	1
		1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0	1
	WRITE	V V V	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	1, 3

Notes: 1. Internal READ and WRITE operations start at the same point in time for BC4 as they do for BL8.
2. Z = Data and strobe output drivers are in tri-state.
3. V = A valid logic level (0 or 1), but the respective input buffer ignores level-on input pins.
4. X = “Don’t Care.”

3 Operating Conditions and Interface Specification

3.1 Absolute Maximum Ratings

Table 12 - Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Note
		Min.	Max.		
Voltage on V_{DD} ball relative to V_{SS}	V_{DD}	–0.4	+1.975	V	1)
Voltage on V_{DDQ} ball relative to V_{SS}	V_{DDQ}	–0.4	+1.975	V	
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	–0.4	+1.975	V	
Storage Temperature	T_{STG}	–55	+150	℃	

1) V_{DD} and V_{DDQ} must be within 300mV of each other at all times. V_{REF} must not be greater than 0.6 x V_{DDQ}. When V_{DD} and V_{DDQ} are less than 500 mV, V_{REF} may be equal or less than 300 mV.

3.2 Operating Conditions

Table 13 - SDRAM Component Operating Temperature Range

Parameter	Symbol	Rating		Unit	Note
		Min.	Max.		
Operating Temperature Range	T_c	0	85	℃	1)2)3)4)
		85	95	℃	1)2)3)4)

1) AX operating case temperature TC is measured in the center of the package, as shown below.
2) A thermal solution must be designed to ensure that the device does not exceed the maximum TC during operation.
3) Device functionality is not guaranteed if the device exceeds maximum TC during operation.
4) If TC exceeds 85°C, the DRAM must be refreshed externally at 2x refresh, which is a 3.9µs interval refresh rate. The use of self refresh temperature (SRT) or automatic self refresh (ASR), must be enabled.

Table 14 - DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{DD}	1.283	1.35	1.45	V	1-7
Supply Voltage for Output	V_{DDQ}	1.283	1.35	1.45	V	1-7
Reference Voltage for DQ, DM inputs	$V_{REFDQ.DC}$	0.49 x V_{DD}	0.5 x V_{DD}	0.51 x V_{DD}	V	8)9)
Reference Voltage for ADD, CMD inputs	$V_{REFCA.DC}$	0.49 x V_{DD}	0.5 x V_{DD}	0.51 x V_{DD}	V	9)10)
External Calibration Resistor connected from ZQ ball to ground	R_{ZQ}	237.6	240.0	242.4	Ω	11)

1) VDD and VDDQ must track one another. VDDQ must be ≤ VDD. VSS = VSSQ.
2) VDD and VDDQ may include AC noise of ±50mV (250 kHz to 20 MHz) in addition to the DC (0 Hz to 250 kHz) specifications. VDD and VDDQ must be at same level for valid AC timing parameters.
3) Maximum DC value may not be greater than 1.425V. The DC value is the linear average of VDD/VDDQ(t) over a very long period of time (for example, 1 second)
4) Under these supply voltages, the device operates to this DDR3 specification
5) If the maximum limit is exceeded, input levels shall be governed by DDR3specifications.
6) Under 1.5V operation, this DDR3 device operates in accordance with the DDR3 specifi-cations under the same speed timings as defined for this device.
7) Once initialized for DDR3 operation, DDR3 operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3 operation (see VDD Voltage Switch-ing .
8) VREFCA(DC) is expected to be approximately 0.5 × VDD and to track variations in the DC level. Externally generated peak noise (non-common mode) on VREFCA may not exceed ±1% × VDD around the VREFCA(DC) value. Peak-to-peak AC noise on VREFCA should not ex-ceed ±2% of VREFCA(DC).
9) DC values are determined to be less than 20 MHz in frequency. DRAM must meet specifi-cations if the DRAM induces additionalAC noise greater than 20 MHz in frequency
10) VREFDQ(DC) is expected to be approximately 0.5 × VDD and to track variations in the DC level. Externally generated peak noise (non-common mode) on VREFDQ maynot exceed ±1% × VDD around the VREFDQ(DC) value. Peak-to-peak AC noise on VREFDQ should not ex-ceed ±2% of VREFDQ(DC).
11) The external calibration resistor R_{ZQ} can be time-shared among DRAMs in multi-rank DIMMs.

Table 15 - Input and Output Leakage Currents

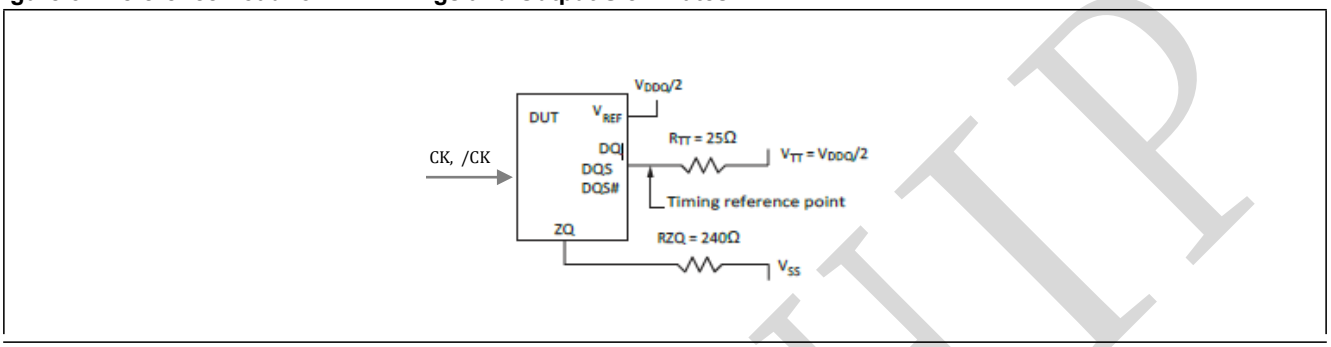
Parameter	Symbol	Condition	Rating		Unit	Note
			Min.	Max.		
Input Leakage Current	I_{IL}	Any input 0 V < V_{IN} < V_{DD}	–2	+2	µA	1)2)
Output Leakage Current	I_{OL}	0V < V_{OUT} < V_{DDQ}	–5	+5	µA	2)3)

1) All other pins not under test = 0 V.
2) Values are shown per ball.
3) DQ's, DQS, /DQS and ODT are disabled.

3.3 Interface Test Conditions

Figure 4 represents the effective reference load of 25 Ω used in defining the relevant timing parameters of the device as well as for output slew rate measurements. It is not intended as either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

Figure 3 - Reference Load for AC Timings and Output Slew Rates



The Timing Reference Points are the idealized input and output nodes / terminals on the outside of the packaged SDRAM device as they would appear in a schematic or an IBIS model.

The output timing reference voltage level for single ended signals is the cross point with $V_{TT.}$

The output timing reference voltage level for differential signals is the cross point of the true (e.g. DQS) and the complement (e.g. /DQS) signal.

3.4 Voltage Levels

3.4.1 DC and AC Logic Input Levels

Single-Ended Signals

Table 16 shows the input levels for single-ended input signals.

Table 16 - DC and AC Input Levels for Single-Ended Command, Address and Control Signals

Parameter	Symbol	DDR3-1600,-1866,-2133		Unit	Note
		Min.	Max.		
DC input logic high	$V_{IH.CA.DC}$	V_{REF} + 0.100	V_{DD}	V	1)
DC input logic low	$V_{IL.CA.DC}$	V_{SS}	V_{REF} - 0.100	V	1)
AC input logic high	$V_{IH.CA.AC}$	V_{REF} + 0.175	See 2)	V	1)
AC input logic low	$V_{IL.CA.AC}$	See 2)	V_{REF} - 0.175	V	1)

1) For input only pins except RESET: $V_{REF} = V_{REF.CA}$
2) See **Chapter 3.9**, **Overshoot and Undershoot Specification**.

Table 17 - DC and AC Input Levels for Single-Ended DQ and DM Signals

Parameter	Symbol	DDR3-1600,-1866,-2133		Unit	Note
		Min.	Max.		
DC input logic high	$V_{IH.DQ.DC}$	V_{REF} + 0.100	V_{DD}	V	1)
DC input logic low	$V_{IL.DQ.DC}$	V_{SS}	V_{REF} - 0.100	V	1)
AC input logic high	$V_{IH.DQ.AC}$	V_{REF} + 0.150	See 2)	V	1) 3)
AC input logic low	$V_{IL.DQ.AC}$	See 2)	V_{REF} - 0.150	V	1) 3)

1) For DQ and DM: $V_{REF} = V_{REFDQ}$, for input only signals except RESET: $V_{REF} = V_{REFCA}$
2) See **Chapter 3.9**, **Overshoot and Undershoot Specification**.
3) Single ended swing requirement for DQS, /DQS is 350 mV (peak to peak). Differential swing requirement for DQS, /DQS is 700 mV (peak to peak).

Differential Swing Requirement for Differential Signals

Table 18 shows the input levels for differential input signals.

Table 18 - Differential swing requirement for clock (CK - /CK) and strobe (DQS - /DQS)

Parameter	Symbol	DDR3-1600,-1866,-2133		Unit	Note
		Min.	Max.		
Differential input high	$V_{IH.DIFF}$	+0.18	See [1]	V	[2]
Differential input low	$V_{IL.DIFF}$	See[1]	–0.18	V	[2]
Differential input high AC	$V_{IH.DIFF.AC}$	2 x ($V_{IH.AC}$ - V_{REF}) [3]	See [1]	V	[4]
Differential input low AC	$V_{IL.DIFF.AC}$	See [1]	2 x (V_{REF} - $V_{IL.AC}$) [5]	V	[4]

1) These values are not defined, however they single-ended signals CK, /CK, DQS, /DQS need to be within the respective limits ($V_{IH.DC.MAX}$, $V_{IL.DC.MIN}$) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to **Chapter 3.9** .
2) Used to define a differential signal slew-rate.
3) Clock: use $V_{IH.CA.AC}$ for $V_{IH.AC}$. Strobe: use $V_{IH.DQ.AC}$ for $V_{IH.AC}$.
4) For CK - /CK use $V_{IH}/V_{IL.AC}$ of ADD/CMD and V_{REFCA}; for DQS - /DQS use $V_{IH}/V_{IL.AC}$ of DQs and V_{REFDQ}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
5) Clock: use $V_{IL.CA.AC}$ for $V_{IL.AC}$. Strobe: use $V_{IL.DQ.AC}$ for $V_{IL.AC}$.

Table 19 - Allowed Time Before Ringback (tDVAC) for CK - /CK and DQS - /DQS

Slew Rate [V/ns]	t_{DVAC} [ps]@ $\|V_{IH/IL.DIFF.AC}\|$		t_{DVAC} [ps]@ $\|V_{IH/IL.DIFF.AC}\|$		
	DDR3-1600		DDR3-1866		
	320mv	270mv	270mv	260mv	250mv
> 4.0	189	201	163	176	168
4.0	189	201	163	176	168
3.0	162	179	140	154	147
2.0	109	134	95	111	105
1.8	91	119	80	97	91
1.6	69	100	62	78	74
1.4	40	76	37	55	52
1.2	Note1	44	5	24	22
1.0	Note1				
<1.0	Note1				

Note:1.Rising input signal shall become equal to or grater than $V_{IH.AC}$ level and failing input signal shall become equal to or less than $V_{IL.AC}$ level.

Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (CK, DQS, /CK, /DQS,) has also to comply with certain requirements for single-ended signals.

CK and /CK have to approximately reach $V_{SEH.MIN}$ / $V_{SEL.MAX}$ (approximately equal to the ac-levels ($V_{IH.AC}$ / $V_{IL.AC}$) for ADD/CMD signals) in every half-cycle

DQS, /DQS have to reach $V_{SEH.MIN}$ / $V_{SEL.MAX}$ (approximately the ac-levels ($V_{IH.AC}$ / $V_{IL.AC}$) for DQ signals) in every half-cycle preceeding and following a valid transition.

Note that the applicable ac-levels for ADD/CMD and DQs might be different per speed-bin etc. E.g. if $V_{IH150.AC}$ / $V_{IL150.AC}$ is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and /CK.

Note that while ADD/CMD and DQ signal requirements are with respect to V_{ref}, the single-ended components of differential signals have a requirement with respect to V_{DD}/2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time.

For single-ended components of differential signals the requirement to reach $V_{SEL.MAX}$, $V_{SEH.MIN}$ has no bearing on timing, but

adds a restriction on the common mode charateristics of these signals.

Table 20 - Each Single-Ended Levels for CK, DQS, /DQS, /CK,

Parameter	Symbol	DDR3-1600,-1866,-2133		Unit	Note
		Min.	Max.		
Single-ended highlevel for strobes	V_{SEH}	(VDD/2) + 160	V_{DDQ}	mV	1,2
Single-ended high-level for CK, /CK	V_{SEH}	(VDD/2) + 160	V_{DD}	mV	
Single-ended low-level for strobes	V_{SEL}	V_{SSQ}	(VDD/2) -0.175	mV	
Single-ended low-level for CK, /CK	V_{SEL}	V_{SS}	(VDD/2) - 0.175	mV	

Note:
1. For CK, CK use VIH/VIL(AC) of address/command; for strobes (DQS, DQS) use VIH/VIL(AC) of DQs.
2. VIH(AC)/VIL(AC) for DQs is based on VREFDQ; VIH(AC)/VIL(AC) for address/command is based on VREFCA; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.

Table 21 - Cross Point Voltage for Differential Input Signals (CK, DQS)

Symbol	Parameter	DDR3-1600,-1866,-2133		Unit	Note
		Min	Max		
V_{IX}	Differential Input Cross Point Voltage relative to VDD/2 for CK, /CK	$V_{REF(DC)}$ –150	$V_{REF(DC)}$+150	mV	1)2)3)
V_{IX}	Differential Input Cross Point Voltage relative to VDD/2 for DQS, DQS	$V_{REF(DC)}$–150	$V_{REF(DC)}$+150	mV	1)2)3)1)

1. Minimum DC limit is relative to single-ended signals; overshoot specifications are appli-cable
2. The typical value of $V_{IX(AC)}$ is expected to be about 0.5 × V_{DD} of the transmitting device, and $V_{IX(AC)}$ is expected to track variations in V_{DD}. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.
3. V_{IX} must provide 25mV (single-ended) of the voltages separation.

3.4.2 DC and AC Output Measurements Levels

Table 22 - DC and AC Output Levels for Single-Ended Signals

Parameter	Symbol	Value	Unit	Note
DC output high measurement level (for output impedance measurement)	$V_{OH.DC}$	0.8 x V_{DDQ}	V	1)2)3)
DC output mid measurement level (for output impedance measurement)	$V_{OM.DC}$	0.5 x V_{DDQ}	V	1)2)3)
DC output low measurement level (for output impedance measurement)	$V_{OL.DC}$	0.2 x V_{DDQ}	V	1)2)3)
AC output high measurement level (for output slew rate)	$V_{OH.AC}$	V_{TT} + 0.1 x V_{DDQ}	V	1)2)3)4)
AC output low measurement level (for output slew rate)	$V_{OL.AC}$	V_{TT} - 0.1 x V_{DDQ}	V	1)2)3)4)

1) RZQ of 240Ω ±1% with RZQ/7 enabled (default 34Ω driver) and is applicable after prop-er ZQ calibration has been performed at a stable temperature and voltage (VDDQ= VDD; VSSQ= VSS).
2) VTT= VDDQ/2.
3) LV curve linearity. Do not use AC test load.
4) See Slew Rate Definitions for Single-Ended Output Signals for output slew-rate.

Table 23 - AC Output Levels for Differential Signals

Parameter	Symbol	Value		Unit	Note
		Min.	Max.		
AC differential output high measurement level (for output slew rate)	$V_{OH.DIFF.AC}$	+0.2 x V_{DDQ}		V	1) 2)
AC differential output low measurement level (for output slew rate)	$V_{OL.DIFF.AC}$	–0.2 x V_{DDQ}		V	1) 2)
Deviation of the output cross point voltage from the termination voltage	V_{OX}	-100	100	mV	3)

1) RZQ of 240Ω ±1% with RZQ/7 enabled (default 34Ω driver) and is applicable after prop-er ZQ calibration has been performed at a stable temperature and voltage (V_{DDQ}= V_{DD}; V_{SSQ}= V_{SS}).

2) The test load configuration.
3) For a differential slew rate between the list values, the $V_{OX(AC)}$ value may be obtained by linear interpolation.

3.5 Output Slew Rates

Table 24 - Output Slew Rates

Parameter	Symbol	DDR3-1600,-1866,-2133		Unit	Note
		Min.	Max.		
Single-ended Output Slew Rate	SRQse	1.75	6	V / ns	1)2)3)4)
Differential Output Slew Rate	SRQdiff	3.5	12	V / ns	

1) RZQ of 240Ω ±1% with RZQ/7 enabled (default 34Ω driver) and is applicable after prop-er ZQ calibration has been performed at a stable temperature and voltage (VDDQ= VDD; VSSQ= VSS)..
2) VTT= VDDQ/2.
3) The test load configuration.
4) The 6 V/ns maximum is applicable for a single DQ signal when it is switching either from HIGH to LOW or LOW to HIGH while the remaining DQ signals in the same byte lane are either all static or all switching in the opposite direction. For all other DQ signal switch-ing combinations, the maximum limit of 6 V/ns is reduced to 5 V/ns.

3.6 ODT DC Impedance and Mid-Level Characteristics

Table 25 provides the ODT DC impedance and mid-level characteristics.

Table 25 - ODT DC Impedance and Mid-Level Characteristics

Symbol	Description	V_{OUT} Condition	Min.	Nom.	Max.	Unit	Note
R_{TT120}	R_{TT} effective = 120 Ω	$V_{IL.AC}$ and $V_{IH.AC}$	0.9	1.0	1.65	R_{ZQ}/2	1)2)3)4)
R_{TT60}	R_{TT} effective = 60 Ω		0.9	1.0	1.65	R_{ZQ}/4	1)2)3)4)
R_{TT40}	R_{TT} effective = 40 Ω		0.9	1.0	1.65	R_{ZQ}/6	1)2)3)4)
R_{TT30}	R_{TT} effective = 30 Ω		0.9	1.0	1.65	R_{ZQ}/8	1)2)3)4)
R_{TT20}	R_{TT} effective = 20 Ω		0.9	1.0	1.65	R_{ZQ}/12	1)2)3)4)
ΔV_M	Deviation of V_M with respect to V_{DDQ} / 2	floating	–5	-	+5	%	1)2)3)4)5)

1) With R_{ZQ} = 240 Ω.
2) Measurement definition for R_{TT} : Apply $V_{IH.AC}$ and $V_{IL.AC}$ to test ball separately, then measure current I ($V_{IH.AC}$) and I ($V_{IL.AC}$) respectively. R_{TT} = [$V_{IH.AC}$ - $V_{IL.AC}$] / [I ($V_{IH.AC}$) - I ($V_{IL.AC}$)]
3) The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see the **ODT DC Impedance Sensitivity on Temperature and Voltage Drifts**.
4) The tolerance limits are specified under the condition that V_{DDQ} = V_{DD} and that V_{SSQ} = V_{SS}.
5) Measurement Definition for ΔV_M: Measure voltage (V_M) at test ball (midpoint) with no load: ΔV_M = (2 × V_M / V_{DDQ} - 1) × 100%

3.7 ODT DC Impedance Sensitivity on Temperature and Voltage Drifts

If temperature and/or voltage change after calibration, the tolerance limits widen for R_{TT} according to the following tables. The following definitions are used:
ΔT = T - T (at calibration)
ΔV = V_{DDQ}- V_{DDQ} (at calibration)
V_{DD} = V_{DDQ}

Table 26 - ODT DC Impedance after proper IO Calibration and Voltage/Temperature Drift

Symbol	Value		Unit	Note
	Min.	Max.		
R_{TT}	0.9 - dR_{TT}dT x |ΔT| - dR_{TT}dV x |ΔV|	1.6 + dR_{TT}dT x |ΔT| + dR_{TT}dV x |ΔV|	R_{ZQ} / $TISF_{RTT}$	1)

Table 27 - OTD DC Impedance Sensitivity Parameters

Symbol	Value		Unit	Note
	Min.	Max.		
$dR_{TT}dT$	0	1.5	%/°C	1)
$dR_{TT}dV$	0	0.15	%/mV	

3.8 Interface Capacitance

Definition and values for interface capacitances are provided in the following table.

Table 28 - Interface Capacitance Values

Parameter	Symbol	DDR3-1600		DDR3-1866,-2133		Unit	Note
		Min.	Max.	Min.	Max.		
Input/Output Capacitance (DQ,DM,DQS,/DQQS)	C_{IO}	1.4	2.2	1.4	2.1	pF	2
Input Capacitance (CK and /CK)	C_{CK}	0.8	1.4	0.8	1.3	pF	
Input Capacitance Delta (CK and /CK)	C_{DCK}	0	0.15	0	0.15	pF	
Input/Output Capacitance delta (DQS and /DQS)	C_{DDQS}	0	0.15	0	0.15	pF	3
Input Capacitance (CK and /CK) (All other input-only pins)	C_I	0.75	1.2	0.75	1.2	pF	5
Input Capacitance delta (All control input-only pins)	C_{DI_CTRL}	-0.4	0.2	-0.4	0.2	pF	6
Input Capacitance delta (All ADD and CMD input-only pins)	$C_{DI\_ADD\_CMD}$	–0.4	0.4	–0.4	0.4	pF	7
Input/Output Capacitance delta (DQ,DM,DQS,/DQQS)	C_{DIO}	-0.5	0.3	-0.5	0.3	pF	4
Input/output capacitance of ZQ pin	C_{ZQ}	–	3	–	3	pF	
Reset pin capacitance	*CRE*	–	3.0	–	3.0	pF	

1. V_{DD} = 1.35V (1.283–1.45V), V_{DDQ} = V_{DD}, V_{REF} = V_{SS}, *f* = 100 MHz, T_C = 25°C. $V_{OUT(DC)}$ = 0.5 × V_{DDQ}, V_{OUT} = 0.1V (peak-to-peak).
2. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
3. Includes .C_{DDQS} is for DQS vs. DQS# separately.
4. C_{DIO} = $C_{IO(DQ)}$ - 0.5 × ($C_{IO(DQS)}$ + $C_{IO(DQS\#)}$).
5. Excludes CK, CKB; CTRL = ODT, CSB, and CKE; CMD = RASB, CASB, and WEB; ADDR = A[*n*:0], BA[2:0].
6. C_{DI_CTRL} = $C_{I(CTRL)}$ - 0.5 × ($C_{CK(CK)}$ + $C_{CK(CKB)}$).
7. $C_{DI\_CMD\_ADDR}$ = $C_{I(CMD\_ADDR)}$ - 0.5 × ($C_{CK(CK)}$ + $C_{CK(CKB)}$).

3.9 Overshoot and Undershoot Specification

Table 29 - AC Overshoot / Undershoot Specification for Address and Control Signals

Parameter	DDR3-1600	DDR3-1866	DDR3-1866	Unit	Note
Maximum peak amplitude allowed for overshoot area	0.4	0.4	0.4	V	1)
Maximum peak amplitude allowed for undershoot area	0.4	0.4	0.4	V	1)
Maximum overshoot area above V_{DD}	0.33	0.28	0.25	V /ns	1)
Maximum undershoot area below V_{SS}	0.33	0.28	0.25	V / ns	1)

1) Applies for the following signals: A[15:0], BA[3:0], /CS, /RAS, /CAS, /WE, CKE and ODT

Figure 4 - AC Overshoot / Undershoot Definitions for Address and Control Signals

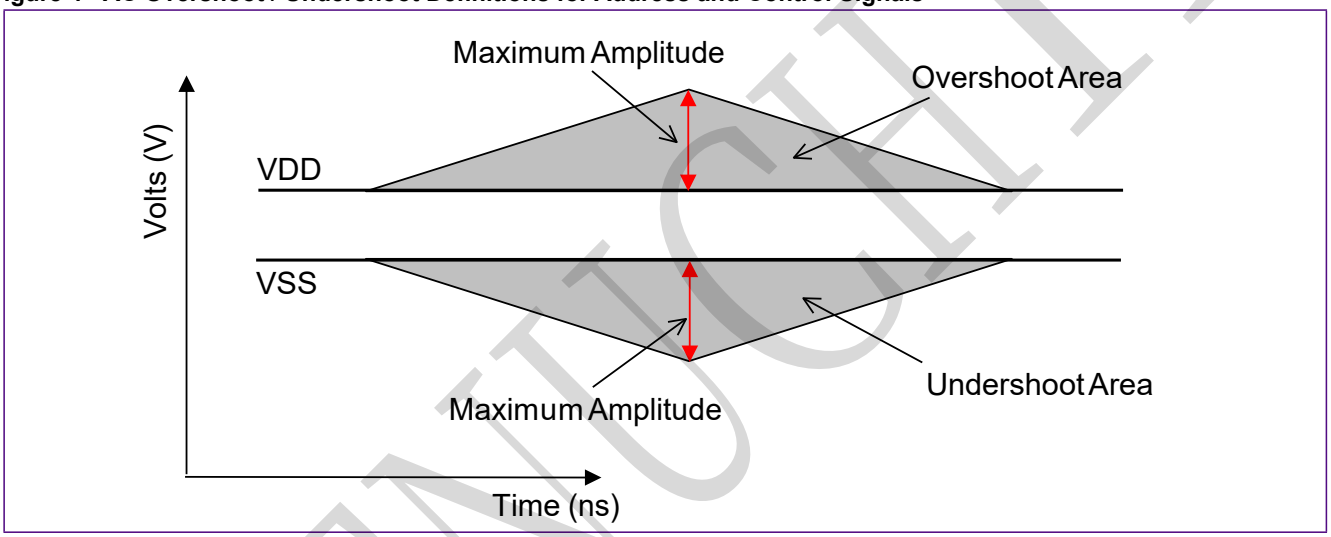
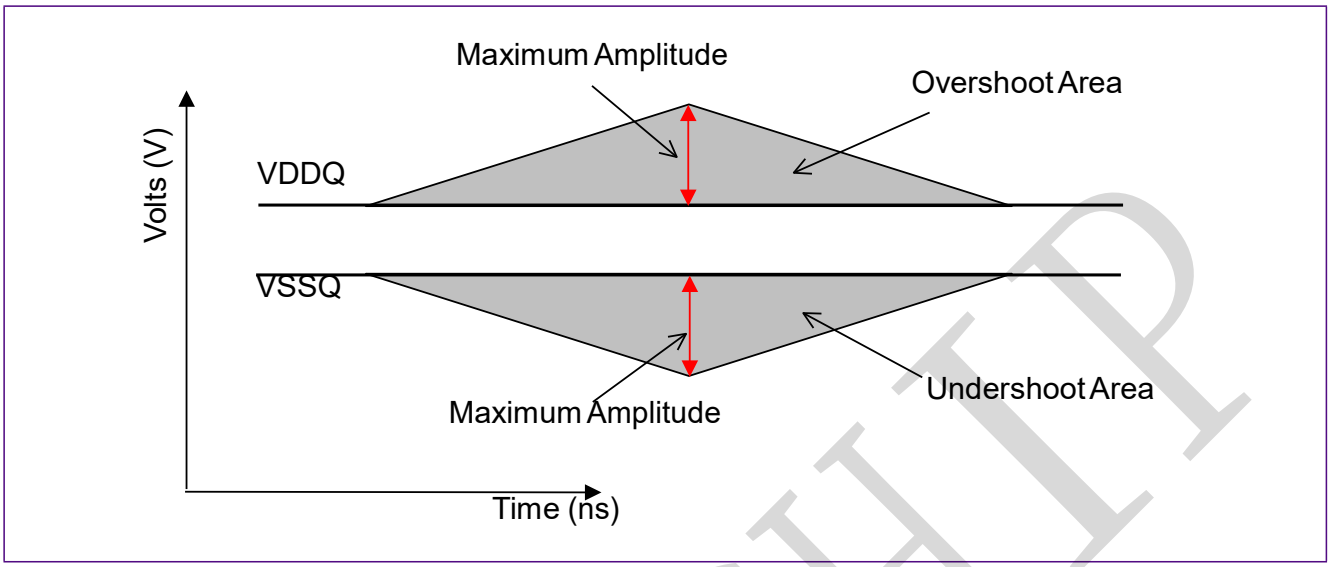


Table 30 - AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask Signals

Parameter	DDR3-1600	DDR3-1866	DDR3-2133	Unit	Note
Maximum peak amplitude allowed for overshoot area	0.4	0.4	0.4	V	1)
Maximum peak amplitude allowed for undershoot area	0.4	0.4	0.4	V	1)
Maximum overshoot area above V_{DDQ}	0.13	0.11	0.1	V /ns	1)
Maximum undershoot area below V_{SSQ}	0.13	0.11	0.1	V / ns	1)

1) Applies for CK, /CK, DQ, DQS, /DQS & DM

Figure 5 - AC Overshoot / Undershoot Definitions for Clock, Data, Strobe and Mask Signals



4 Speed Bins, AC Timing and IDD

The following AC timings are provided with CK AND /CK and DQS AND /DQS differential slew rate of 2.0 V/ns. Timings are further provided for calibrated OCD drive strength under the “Reference Load for Timing Measurements” according to **Chapter 3.3** only.

The CK AND /CK input reference level (for timing referenced to CK AND /CK) is the point at which CK and /CK cross. The DQS AND /DQS reference level (for timing referenced to DQS AND /DQS) is the point at which DQS and /DQS cross. The output timing reference voltage level is V_{TT}.

4.1 Speed Bins

The following tables show DDR3 speed bins and relevant timing parameters. Other timing parameters are provided in the following chapter. For availability and ordering information of products for a specific speed bin, please see **Table 1**.

General Notes for Speed Bins:

- The CL setting and CWL setting result in $t_{CK.AVG.MIN}$ and $t_{CK.AVG.MAX}$ requirements. When making a selection of $t_{CK.AVG}$, both need to be fulfiled: Requirements from CL setting as well as requirements from CWL setting
- $t_{CK.AVG.MIN}$ limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller industry standard $t_{CK.AVG}$ value (2.5, 1.875, 1.5) when calculating CL [nCK] = t_{AA} [ns] / $t_{CK.AVG}$ [ns], rounding up to the next ‘Supported CL’
- $t_{CK.AVG.MAX}$ limits: Calculate $t_{CK.AVG}$ = $t_{AA.MAX}$ / CLSELECTED and round the resulting $t_{CK.AVG}$ down to the next valid speed bin limit (i.e. 3.3 ns or 2.5 ns or 1.875 ns or 1.25 ns). This result is $t_{CK.AVG.MAX}$ corresponding to

The absolute specification for all speed bins is T_{OPER} and V_{DD} = V_{DDQ} = 1.283V to 1.45V In addition the following general notes apply.

CLSELECTED ‘Reserved’ settings are not allowed. User must program a different value

- Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the tables which are not subject to Production Tests but verified by Design/Characterization
- Any DDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the tables which are not subject to Production Tests but verified by Design/Characterization

Table 31 - DDR3-1600 Speed Bins

Speed Bin				**DDR3-1600**		**Unit**	**Note**
CL-t_{RCD}-t_{RP}				**11-11-11**			
Parameter			**Symbol**	**Min.**	**Max.**		
Internal read command to first data			tAA	13.75	—	ns	
Active to read or write delay time			tRCD	13.75	—	ns	
Pre-charge command period			tRP	13.75	—	ns	
Active to active/auto-refresh command time			tRC	48.75	—	ns	
Active to pre-charge command period			tRAS	35	9*tREFI	ns	1
Average Clock Cycle Time	CL=5	CWL=5	tCK(avg)	3.0	3.3	ns	2
		CWL=6,7,8	tCK(avg)	Reserved	Reserved	ns	3
	CL=6	CWL=5	tCK(avg)	2.5	3.3	ns	2
		CWL=6,7,8	tCK(avg)	Reserved	Reserved	ns	3
	CL=7	CWL=5，7,8	tCK(avg)	Reserved	Reserved	ns	3
		CWL=6	tCK(avg)	1.875	＜2.5	ns	2
	CL=8	CWL=5,7,8	tCK(avg)	Reserved	Reserved	ns	3
		CWL=6	tCK(avg)	1.875	＜2.5	ns	2
	CL=9	CWL=5,6,8	tCK(avg)	Reserved	Reserved	ns	3
		CWL=7	tCK(avg)	1.5	＜1.875	ns	2
	CL=10	CWL=5,6,8	tCK(avg)	Reserved	Reserved	ns	3
		CWL=7	tCK(avg)	1.5	＜1.875	ns	2
		CWL=8	tCK(avg)	Reserved	Reserved	ns	3
	CL=11	CWL=5,6,7	tCK(avg)	Reserved	Reserved	ns	3
		CWL=8	tCK(avg)	1.25	＜1.5	ns	2
Supported CL setting				5,6,7,8，9,10,11		CK	
Supported CWL setting				5,6,7,8		CK	

Table 32 - DDR3-1866 Speed Bins

Speed Bin				**DDR3-1866**		**Unit**	**Note**
CL-t_{RCD}-t_{RP}				**13-13-13**			
Parameter			**Symbol**	**Min.**	**Max.**		
Internal read command to first data			tAA	13.91	20.0	ns	
Active to read or write delay time			tRCD	13.91	—	ns	
Pre-charge command period			tRP	13.91	—	ns	
Active to active/auto-refresh command time			tRC	47.91 (47.125))	—	ns	
Active to pre-charge command period			tRAS	34	9*tREFI	ns	1
Average Clock Cycle Time	CL=5	CWL=5	tCK(avg)	3.0	3.3	ns	2
		CWL=6,7,8,9	tCK(avg)	Reserved	Reserved	ns	3
	CL=6	CWL=5	tCK(avg)	2.5	3.3	ns	2
		CWL=6,7,8,9	tCK(avg)	Reserved	Reserved	ns	3
	CL=7	CWL=5,7,8,9	tCK(avg)	Reserved	Reserved	ns	3
		CWL=6	tCK(avg)	1.875	＜2.5	ns	2
	CL=8	CWL=5,7,8,9	tCK(avg)	Reserved	Reserved	ns	3
		CWL=6	tCK(avg)	1.875	＜2.5	ns	2
	CL=9	CWL=5,6,8,9	tCK(avg)	Reserved	Reserved	ns	3
		CWL=7	tCK(avg)	1.5	＜1.875	ns	2
	CL=10	CWL=5,6,8,9	tCK(avg)	Reserved	Reserved	ns	3
		CWL=7	tCK(avg)	1.5	＜1.875	ns	2
	CL=11	CWL=5,6,7,9	tCK(avg)	Reserved	Reserved	ns	3
		CWL=8	tCK(avg)	1.25	＜1.5	ns	2
	CL=12	CWL=5~8	tCK(avg)	Reserved	Reserved	ns	3
		CWL=9	tCK(avg)	Reserved	Reserved	ns	2
	CL=13	CWL=5~8	tCK(avg)	Reserved	Reserved	ns	2
		CWL=9	tCK(avg)	1.07	＜1.25	ns	2
Supported CL setting				5,6,7,8,9,10,11,13		CK	
Supported CWL setting				5,6,7,8		CK	

Table 33 - DDR3-2133 Speed Bins

Speed Bin				**DDR3-2133**		**Unit**	**Note**
CL-t_{RCD}-t_{RP}				**14-14-14**			
Parameter			**Symbol**	**Min.**	**Max.**		
Internal read command to first data			tAA	13.09	20.0	ns	
Active to read or write delay time			tRCD	13.09	—	ns	
Pre-charge command period			tRP	13.09	—	ns	
Active to active/auto-refresh command time			tRC	46.09	—	ns	
Active to pre-charge command period			tRAS	33	9*tREFI	ns	1
Average Clock Cycle Time	CL=5	CWL=5	tCK(avg)	3.0	3.3	ns	2
		CWL=6,7,8,9	tCK(avg)	Reserved	Reserved	ns	3
	CL=6	CWL=5	tCK(avg)	2.5	3.3	ns	2
		CWL=6,7,8,9	tCK(avg)	Reserved	Reserved	ns	3
	CL=7	CWL=5,7,8,9	tCK(avg)	Reserved	Reserved	ns	3
		CWL=6	tCK(avg)	1.875	＜2.5	ns	2
	CL=8	CWL=5,7,8,9	tCK(avg)	Reserved	Reserved	ns	3
		CWL=6	tCK(avg)	1.875	＜2.5	ns	2
	CL=9	CWL=5,6,8,9	tCK(avg)	Reserved	Reserved	ns	3
		CWL=7	tCK(avg)	1.5	＜1.875	ns	2
	CL=10	CWL=5,6,8,9	tCK(avg)	Reserved	Reserved	ns	3
		CWL=7	tCK(avg)	1.5	＜1.875	ns	2
	CL=11	CWL=5,6,7,9	tCK(avg)	Reserved	Reserved	ns	3
		CWL=8	tCK(avg)	1.25	＜1.5	ns	2
	CL=12	CWL=5~8	tCK(avg)	Reserved	Reserved	ns	3
		CWL=9	tCK(avg)	Reserved	Reserved	ns	2
	CL=13	CWL=5~8	tCK(avg)	Reserved	Reserved	ns	2
		CWL=9	tCK(avg)	1.07	＜1.25	ns	2
	CL=14	CWL=5~9	tCK(avg	Reserved	Reserved	ns	2
		CWL=10	tCK(avg	0.938	＜107	ns	2
Supported CL setting				5,6,7,8,9,10,11,13,14		CK	
Supported CWL setting				5,6,7,8,9		CK	

Note:

1.all voltages are referenced to Vss;

2.Output timings are only valid for RON34 output buffer selection.

3.The unit tCK (AVG) represents the actual tCK (AVG) of the input clock under operation. The unit CK represents one clock cycle of the input clock, counting the actual clock edges.

4.2 AC Timing Characteristics (VDD = 1.283V to 1.45V; VDDQ =1.283V to 1.45V)

Table 34 - AC Timing parameters

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133		Max	Note
		Min	Max	Min	Max	Min	Max		
Average clock cycle time	$t_{CK(avg)}$	See Speed Bins Table						ns	10,11
Minimum clock cycle time(DLL-off mode)	t_{CK}	8	-	8	-	8	-	ns	9,42
Average CK high level width	$t_{CH(avg)}$	0.47	0.53	0.47	0.53	0.47	0.53	Ck	12
Average CK low level width	$t_{CL(avg)}$	0.47	0.53	0.47	0.53	0.47	0.53	Ck	12
Active Bank A to Active Bank B command period	t_{RRD}	6ns)	7.5ns	6ns)	7.5ns	6ns)	7.5ns	Ck	31
Four activate window	t_{FAW}	30(1 Kb)	-	27(1 Kb)	-	25(1 Kb)	-	ns	31
		40(2 Kb)	-	35(2 Kb)	-	35(2 Kb)	-	ns	31
Address and Control input hold time (VIH/VIL (DC90) levels)	tIH(base) DC90	130	-	110	-	95	-	ps	29,30
Address and Control input setup time (VIH/VIL (AC125) levels)	t_{IS} AC125	-	-	150	-	135	-	ps	29,30, 44
Address and Control input setup time (VIH/VIL (AC135) levels)	$t_{IS(base)}$ AC135(160)	185(60)	-	65	-	60	-	ps	29,30, 44
DQ and DM input hold time (VIH/VIL (DC) levels)	$t_{DH(base)}$	45	-	70	-	60	-	ps	17
DQ and DM input setup time (VIH/VIL (AC) levels)	$t_{DS(base)}$	10	-	68	-	55	-	ps	17
Control and Address Input pulse width for each input	t_{IPW}	560	-	535	-	470	-	ps	41
DQ and DM Input pulse width for each input	t_{DIPW}	360	-	320	-	280	-	ps	41
DQ high impedance time	$t_{HZ(DQ)}$	-	225	-	195	-	180	ps	22,23
DQ low impedance time	$t_{LZ(DQ)}$	-450	225	-390	195	-360	180	ps	22,23
DQS, DQS high impedance time (RL + BL/2 reference)	$t_{HZ(DQS)}$	-	225	-	195	-	180	ps	22,23
DQS, DQS low impedance time (RL - 1 reference)	$t_{LZ(DQS)}$	-450	225	-390	195	-360	180	ps	22,23
DQS, DQS to DQ Skew, per group, per access	t_{DQSQ}	-	100	-	85	-	75	ps	
CAS to CAS command delay	t_{CCD}	4	-	4	-	4	-	CK	
DQ output hold time from DQS, DQS	t_{QH}	0.38	-	0.38	-	0.38	-	Ck	21
DQS, DQS rising edge output access time from rising CK, CK	t_{DQSCK}	-225	225	-195	195	-195	195	ps	23
DQS latching rising transitions to associated clock edges	t_{DQSS}	-0.27	0.27	-0.27	0.27	-0.27	0.27	Ck	25
DQS falling edge hold time from rising CK	t_{DSH}	0.18	-	0.18	-	0.18	-	Ck	25
DQS falling edge setup time to rising CK	t_{DSS}	0.18	-	0.18	-	0.18	-	Ck	25
DQS input high pulse width	t_{DQSH}	0.45	0.55	0.45	0.55	0.45	0.55	Ck	

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133		Unit	Note
		Min	Max	Min	Max	Min	Max		
DQS input low pulse width	t_{DQSL}	0.45	0.55	0.45	0.55	0.45	0.55	Ck	
DQS output high time	t_{QSH}	0.45	0.55	0.40	0.55	0.40	0.55	Ck	25
DQS output low time	t_{QSL}	0.40	-	0.40	-	0.40	-	Ck	21
Mode register set command cycle time	t_{MRD}	4	-	4	-	4	-	CK	
Mode register set command update delay	t_{MOD}	15	-	15	-	15	-	ns	
Read preamble time	t_{RPRE}	0.9	-	0.9	-	0.9	-	Ck	23,24
Read postamble time	t_{RPST}	0.3	-	0.3	-	0.3	-	Ck	23,27
Write preamble time	t_{WPRE}	0.9	-	0.9	-	0.9	-	Ck	
Write postamble time	t_{WPST}	0.3	-	0.3	-	0.3	-	Ck	
Write recovery time	t_{WR}	15	-	15	-	15	-	ns	31,32, 33
Auto precharge write recovery + Precharge time	$t_{DAL}(min)$	WR +tRP/tCK(AVG)						CK	
Multi-purpose register recovery time	t_{MPRR}	1	-	1	-	1	-	CK	
Internal write to read command delay	t_{WTR}	7.5	-	7.5	-	7.5	-	ns	31,34
Internal read to precharge command delay	t_{RTP}	7.5	-	7.5	-	7.5	-	ns	31,32
Minimum CKE low width for Self-refresh entry to exit timing	t_{CKERE}	$t_{CKE}(min)$ +CK	-	$t_{CKE}(min)$ +CK	-	$t_{CKE}(min)$ +CK	-		
Valid clock requirement after Self- refresh entry or Power-down entry	t_{CKSRE}	10	-	10	-	10	-	ns	
		5	-	5	-	5	-	CK	
Valid clock requirement before Self- refresh exit or Power-down exit	t_{CKSRX}	10	-	10	-	10	-	ns	
		5	-	5	-	5	-	CK	
Exit Self-refresh to commands not requiring a locked DLL	t_{XS}	$t_{RFC}(min)$ +10	-	$t_{RFC}(min)$ +10	-	$t_{RFC}(min)$ +10	-	ns	
		5	-	5	-	5	-	CK	
Exit Self-refresh to commands requiring a locked DLL	t_{XSDLL}	tDLLK (min)	-	tDLLK (min)	-	tDLLK (min)	-	CK	
Auto-refresh to Active/Auto-refresh command time	t_{RFC}	260	-	260	-	260	-	ns	28
Average Periodic Refresh Interval 0°C ≤ Tc ≤ +85°C	t_{REFI}	-	7.8	-	7.8	-	7.8	µs	36
Average Periodic Refresh Interval +85°C < Tc ≤ +95°C	t_{REFI}	-	3.9	-	3.9	-	3.9	µs	36
CKE minimum high and low pulse width	t_{CKE}	5	-	5	-	5	-	ns	
		3	-	3	-	3	-	CK	
Exit reset from CKE high to a valid command	t_{XPR}	tRFC(min) +10	-	$t_{RFC}(min)$ +10	-	$t_{RFC}(min)$ +10	-	ns	
		5	-	5	-	5	-	CK	
DLL locking time	t_{DLLK}	512	-	512	-	512	-	CK	28

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133		Unit	Note
		Min	Max	Min	Max	Min	Max		
Power-down entry to exit time	t_{PD}	t_{CKE}(min)	9*t_{REFI}	t_{CKE}(min)	9*t_{REFI}	t_{CKE}(min)	9*t_{REFI}		
Exit precharge power-down with DLL frozen to commands requiring a locked DLL	t_{XPDLL}	24	-	24	-	24	-	ns	
		10	-	10	-	10	-	CK	28
Exit power-down with DLL on to any valid command; Exit precharge power-down with DLL frozen to commands not requiring a locked DLL	t_{XP}	6	-	6	-	6	-	ns	
		3	-	3	-	3	-	CK	28
Command pass disable delay	t_{CPDED}	1	-	2	-	2	-	CK	
Timing of ACT command to Power-down entry	$t_{ACTPDEN}$	1	-	1	-	1	-	CK	
Timing of PRE command to Power-down entry	t_{PRPDEN}	1	-	1	-	1	-	CK	
Timing of RD/RDA command to Power-down entry	t_{RDPDEN}	RL+4+1	-	RL+4+1	-	RL+4+1	-	CK	
Timing of WR command to Power-down entry (BL8OTF, BL8MRS, BL4OTF)	t_{WRPDEN} (min)	WL + 4 + [tWR/tCK(avg)]						CK	
Timing of WR command to Power-down entry (BC4MRS)	t_{WRPDEN} (min)	WL + 2 + [tWR/tCK(avg)]						CK	
Timing of REF command to Power-down entry	$t_{REFPDEN}$	1	-	1	-	1	-	nCK	37
Timing of MRS command to Power-down entry	$t_{MRSPDEN}$	tMOD(min)	-	tMOD (min)	-	tMOD (min)	-		
RTT turn-on	t_{AON}	-225	225	-195	195	-180	180	ps	23,38
Asynchronous RTT turn-on delay (Power-down with DLL frozen)	t_{AONPD}	2	8.5	2	8.5	2	8.5	ns	38
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	t_{AOF}	0.3	0.7	0.3	0.7	0.3	0.7	Ck	39,40
Asynchronous RTT turn-off delay (Power-down with DLL frozen)	t_{AOFPD}	2	8.5	2	8.5	2	8.5	ns	40
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	4	-	CK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	CK	
RTT dynamic change skew	t_{ADC}	0.3	0.7	0.3	0.7	0.3	0.7	Ck	39
Power-up and reset calibration time	t_{ZQinit}	512	-	512	-	512	-	CK	
Normal operation full calibration time	t_{ZQoper}	256	-	256	-	256	-	CK	
Normal operation short calibration time	t_{ZQCS}	64	-	64	-	64	-	CK	
First DQS pulse rising edge after write leveling mode is programmed	t_{WLMRD}	40	-	40	-	40	-	CK	

Parameter	Symbol	DDR3-1600		DDR3-1866		DDR3-2133		Unit	Note
		Min	Max	Min	Max	Min	Max		
DQS, DQS delay after write leveling mode is pro-grammed	$t_{WLDQSEN}$	25	-	25	-	25	-	CK	
Write leveling setup time from risingCK,CK crossing to rising DQS, DQS crossing	t_{WLS}	165	-	140	-	125	-	ps	
Write leveling hold time from rising DQS, DQS crossing to rising CK, CK crossing	t_{WLH}	165	-	140	-	125		ps	
Write leveling output delay	t_{WLO}	0	7.5	0	7.5	0	7	ns	
Write leveling output error	t_{WLOE}	0	2	0	2	0	2	ns	
Absolute clock period	$t_{CK}(abs)$	tCK(avg)min + tJIT(per)min	tCK(avg)max +tJIT(per)max	tCK(avg)min +tJIT(per)min	tCK(avg)max +tJIT(per)max	tCK(avg)min +tJIT(per)min	tCK(avg)max +tJIT(per)max	ps	
Absolute clock high pulse width	$t_{CH}(abs)$	0.43	-	0.43	-	0.43	-	Ck	30
Absolute clock low pulse width	$t_{CL}(abs)$	0.43	-	0.43	-	0.43	-	Ck	31
Clock period jitter	$t_{JIT}(per)$	-70	70	-60	60	-50	50	ps	
Clock period jitter during DLL locking period	$t_{JIT}(per,lck)$	-60	60	-50	50	-40	40	ps	
Cycle to cycle period jitter	$t_{JIT}(cc)$	140		120		120		ps	
Cycle to cycle period jitter during DLL locking period	$t_{JIT}(cc,lck)$	120		100		100		ps	
Cumulative error across 2 cycles	$t_{ERR}(2per)$	-103	103	-88	88	-74	74	ps	17
Cumulative error across 3 cycles	$t_{ERR}(3per)$	-122	122	-105	105	-87	87	ps	17
Cumulative error across 4 cycles	$t_{ERR}(4per)$	-136	136	-117	117	-97	97	ps	17
Cumulative error across 5 cycles	$t_{ERR}(5per)$	-147	147	-126	126	-105	105	ps	17
Cumulative error across 6 cycles	$t_{ERR}(6per)$	-155	155	-133	133	-111	111	ps	17
Cumulative error across 7 cycles	$t_{ERR}(7per)$	-163	163	-139	139	-116	116	ps	17
Cumulative error across 8 cycles	$t_{ERR}(8per)$	-169	169	-145	145	-121	121	ps	17
Cumulative error across 9 cycles	$t_{ERR}(9per)$	-175	175	-150	150	-125	125	ps	17
Cumulative error across 10 cycles	$t_{ERR}(10per)$	-180	180	-154	154	-128	128	ps	17
Cumulative error across 11 cycles	$t_{ERR}(11per)$	-184	184	-158	158	-132	132	ps	17
Cumulative error across 12 cycles	$t_{ERR}(12per)$	-188	188	-161	161	-134	134	ps	17
Cumulative error across n = 13,14,...49,50 cycles	$t_{ERR}(nper)$	$t_{ERR}(nper)min=(1+0.68ln(n))*t_{JIT}(per)min$ $t_{ERR}(nper)max = (1 + 0.68ln(n))*t_{JIT}(per)max$						ps	17

Notes for AC Electrical Characteristics

1. AC timing parameters are valid from specified TC MIN to TC MAX values.
2. All voltages are referenced to VSS.
3. Output timings are only valid for RON34 output buffer selection.
4. The unit tCK (AVG) represents the actual tCK (AVG) of the input clock under operation. The unit CK represents one clock cycle of the input clock, counting the actual clock edges.
5. AC timing and IDD tests may use a VIL-to-VIH swing of up to 900mV in the test environ-ment, but input timing is still referenced to VREF (except tIS, tIH, tDS, and tDH use the AC/DC trip points and CK, CKB and DQS, DQS# use their crossing points). The minimum slew rate for the input signals used to test the device is 1 V/ns for single-ended inputs and 2 V/ns for differential inputs in the range between VIL(AC) and VIH(AC).
6. All timings that use time-based values (ns, µs, ms) should use tCK (AVG) to determine the correct number of clocks uses CK or tCK [AVG] interchangeably). In the case of noninteger results, all minimum limits are to be rounded up to the nearest whole integer, and all maximum limits are to be rounded down to the nearest whole integer.
7. Strobe or DQSdiff refers to the DQS and DQS# differential crossing point when DQS is the rising edge. Clock or CK refers to the CK and CKB differential crossing point when CK is the rising edge.
8. This output load is used for all AC timing (except ODT reference timing) and slew rates. The actual test load may be different. The output signal voltage reference point is VDDQ/2 for single-ended signals and the crossing point for differential signals.
9. When operating in DLL disable mode, PTC does not warrant compliance with normal mode timings or functionality.
10. The clock's tCK (AVG) is the average clock over any 200 consecutive clocks and tCK(AVG) MIN is the smallest clock rate

allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.

11. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20–60 kHz with an additional 1% of tCK (AVG) as a long-term jitter component; however, the spread spectrum may not use a clock rate below tCK (AVG) MIN.
12. The clock's tCH (AVG) and tCL (AVG) are the average half clock period over any 200 con-secutive clocks and is the smallest clock half period allowed, with the exception of a de-viation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
13. The period jitter (tJITper) is the maximum deviation in the clock period from the average or nominal clock. It is allowed in either the positive or negative direction.
14. tCH (ABS) is the absolute instantaneous clock high pulse width as measured from one rising edge to the following falling edge.
15. tCL (ABS) is the absolute instantaneous clock low pulse width as measured from one fall-ing edge to the following rising edge.
16. The cycle-to-cycle jitter tJITcc is the amount the clock period can deviate from one cycle to the next. It is important to keep cycle-to-cycle jitter at a minimum during the DLL locking time.
17. The cumulative jitter error tERRnper, where n is the number of clocks between 2 and 50, is the amount of clock time allowed to accumulate consecutively away from the average clock over n number of clock cycles.
18. tDS (base) and tDH (base) values are for a single-ended 1 V/ns slew rate DQs and 2 V/ns slew rate differential DQS, DQS#; when DQ single-ended slew rate is 2V/ns, the DQS dif-ferential slew rate is 4V/ns.
19. These parameters are measured from a data signal (DM, DQ0, DQ1, and so forth) transi-tion edge to its respective data strobe signal (DQS, DQS#) crossing.
20. The setup and hold times are listed converting the base specification values (to which derating tables apply) to VREF when the slew rate is 1 V/ns. These values, with a slew rate of 1 V/ns, are for referenceonly.
21. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJITper (larger of tJITper (MIN) or tJITper (MAX) of the input clock (output deratings are relative to the SDRAM input clock).
22. Single-ended signal parameter.
23. The DRAM output timing is aligned to the nominal or average clock. Most output pa-rameters must be derated by the actual jitter error when input clock jitter is present, even when within specification. This results in each parameter becoming larger. The fol-lowing parameters are required to be derated by subtracting tERR10per (MAX): tDQSCK (MIN), tLZDQS (MIN), tLZDQ (MIN), and tAON (MIN). The following parameters are re-quired to be derated by subtracting tERR10per (MIN): tDQSCK (MAX), tHZ (MAX), tLZDQS (MAX), tLZDQ MAX, and tAON (MAX). The parameter tRPRE (MIN) is derated by subtract-ing tJITper (MAX), while tRPRE (MAX) is derated by subtracting tJITper (MIN).
24. The maximum preamble is bound by tLZDQS (MAX).
25. These parameters are measured from a data strobe signal (DQS, DQS#) crossing to its re-spective clock signal (CK, CKB) crossing. The specification values are not affected by the amount of clock jitter applied, as these are relative to the clock signal crossing. These parameters should be met whether clock jitter is present.
26. The tDQSCK (DLL_DIS) parameter begins CL + AL - 1 cycles after the READ command.
27. The maximum postamble is bound by tHZDQS (MAX).
28. Commands requiring a locked DLL are: READ (and RDAP) and synchronous ODT com-mands. In addition, after any change of latency tXPDLL, timing must be met.
29. tIS (base) and tIH (base) values are for a single-ended 1 V/ns control/command/address slew rate and 2 V/ns CK, CKB differential slew rate.
30. These parameters are measured from a command/address signal transition edge to its respective clock (CK, CKB) signal crossing. The specification values are not affected by the amount of clock jitter applied as the setup and hold times are relative to the clock signal crossing that latches the command/address. These parameters should be met whether clock jitter is present.
31. For these parameters, the DDR3 SDRAM device supports tnPARAM (nCK) = RU(tPARAM [ns]/tCK[AVG] [ns]), assuming all input clock jitter specifications are satisfied. For exam-ple, the device will support tnRP (nCK) = RU(tRP/tCK[AVG]) if all input clock jitter specifi-cations are met. This means that for DDR3-800 6-6-6, of which tRP = 5ns, the device will support tnRP = RU(tRP/tCK[AVG]) = 6 as long as the input clock jitter specifications are met. That is, the PRECHARGE command at T0 and the ACTIVATE command at T0 + 6 are valid even if six clocks are less than 15ns due to input clock jitter.
32. During READs and WRITEs with auto precharge, the DDR3 SDRAM will hold off the in-ternal PRECHARGE command until tRAS (MIN) has beensatisfied.
33. When operating in DLL disable mode, the greater of 4CK or 15ns is satisfied for tWR.
34. The start of the write recovery time is defined as follows: • For BL8 (fixed by MRS or OTF): Rising clock edge four clock cycles after WL
    • For BC4 (OTF): Rising clock edge four clock cycles after WL
    • For BC4 (fixed by MRS): Rising clock edge two clock cycles afterWL
35. RESET# should be LOW as soon as power starts to ramp to ensure the outputs are in High-Z. Until RESET# is LOW, the outputs are at risk of driving and could result in exces-sive current, depending on busactivity.
36. The refresh period is 64ms when TC is less than or equal to 85°C. This equates to an aver-age refresh rate of 7.8125µs. However, nine REFRESH commands should be asserted at least once every 70.3µs. When TC is greater than 85°C, the refresh period is 32ms.
37. Although CKE is allowed to be registered LOW after a REFRESH command when tREFPDEN (MIN) is satisfied, there are cases where additional time such as tXPDLL (MIN) is required.

38. ODT turn-on time MIN is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time maximum is when the ODT resistance is fully on. The ODT reference load is shown. This output load is used for ODT timings.Designs that were created prior to JEDEC tightening the maxi- mum limit from 9ns to 8.5ns will be allowed to have a 9nsmaximum.
39. Half-clock output parameters must be derated by the actual tERR10per and tJITdtywhen input clock jitter is present. This results in each parameter becoming larger. Theparame-ters tADC (MIN) and tAOF (MIN) are each required to be derated by subtracting both tERR10per (MAX) and tJITdty (MAX). The parameters tADC (MAX) and tAOF (MAX) are required to be derated by subtracting both tERR10per (MAX) and tJITdty (MAX).
40. ODT turn-off time minimum is when the device starts to turn off ODT resistance. ODT turn-off time maximum is when the DRAM buffer is in High-Z. The ODT reference load is shown. This output load is used for ODT timings .
41. Pulse width of a input signal is defined as the width between the first crossing of VREF(DC) and the consecutive crossing of VREF(DC).
42. Should the clock rate be larger than tRFC (MIN), an AUTO REFRESH command should have at least one NOP command between it and another AUTO REFRESH command. Ad-ditionally, if the clock rate is slower than 40ns (25 MHz), all REFRESH commands should be followed by a PRECHARGE ALL command.
43. DRAM devices should be evenly addressed when being accessed. Disproportionate ac-cesses to a particular row address may result in a reduction of REFRESH characteristics or product lifetime.
44. When two VIH(AC) values (and two corresponding VIL(AC) values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one VIH(AC) value may be used for address/command inputs and the other VIH(AC) value may be used for data inputs.

For example, for DDR3-800, two input AC levels are defined: VIH(AC175),min and VIH(AC150),min (corresponding VIL(AC175),min and VIL(AC150),min). For DDR3-800, the address/ command inputs must use either VIH(AC175),min with tIS(AC175) of 200ps or VIH(AC150),min with tIS(AC150) of 350ps; independently, the data inputs must use either VIH(AC175),min with tDS(AC175) of 75ps or VIH(AC150),min with tDS(AC150) of 125ps.

4.3 IDD Specification (IDD Maximum Limits Die for 1.35/1.5V Operation)

Table 35 - IDD Specification

Conditions	Sym	1600	1866	2133	Note
Operating One Bank Active-Precharge Current; CKE: High; External clock: On; tCK, nRC, nRAS, CL: see timing used table; BL: 8; AL: 0; /CS: High between ACT and PRE; Command, Address: partially toggling; Data IO: FLOATING; DM:stable at 0; Bank Activity: Cycling with one bank active at a time; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD0 (x8)	47	49	51	1,2
	IDD0 (x16)	57	59	61	1,2
Operating One Bank Active-Read-Precharge Current; CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see timing used table; BL: 81; AL: 0; /CS: High between ACT, RD and PRE; Com- mand, Address, Data IO: partially toggling; DM:stable at 0; Bank Activity: Cycling with one bank active at a time; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD1 (x8)	61	64	67	1,2
	IDD1 (x16)	81	84	87	1,2
Precharge Power-Down Current Slow Exit; CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Pre-charge Power Down Mode: Slow Exit	IDD2P0	8		1,2	
Precharge Power-Down Current Fast Exit; CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Pre-charge Power Down Mode: Fast Exit	IDD2P1	14	16	18	1,2
Precharge Standby Current; CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD2N	24	26	28	1,2
Precharge Standby ODT Current; CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: tog- gling	IDD2NT (x8)	28	30	32	1,2
	IDD2NT (x16)	31	33	35	1,2
Precharge Quiet Standby Current; CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD2Q	24	26	30	1,2
Active Power-Down Current; CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD3P	26	28	30	1,2
Active Standby Current; CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD3N (x8)	30	32	34	1,2
	IDD3N (x16)	38	40	42	1,2
Operating Burst Read Current; CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: High between RD; Command, Address: par-tially toggling; Data IO: seamless read data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD4R (x8)	95	105	115	1,2
	IDD4R (x16)	155	165	175	1,2

Conditions	Symbol	1600	1866	2133	Note
Operating Burst Write Current; CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; /CS: High between WR; Command, Address: par-tially toggling; Data IO: seamless write data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at HIGH	IDD4W (x8)	95	105	115	1,2
	IDD4W (x16)	155	165	175	1,2
Burst Refresh Current; CKE: High; External clock: On; tCK, CL, nRFC: see timing used table; BL: 8; AL: 0; /CS: High between REF; Command, Address: partially toggling; Data IO: FLOATING; DM:stable at 0; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD5B	175	180	185	1,2
Self Refresh Current: Normal Temperature Range; TCASE: 0- 85°C; Auto Self-Refresh (ASR): Dis- abled; Self-Refresh Temperature Range (SRT): Normal; CKE: Low; External clock: Off; CK and CK: LOW; CL: see timing used table; BL: 8; AL: 0; /CS, Command, Address, Data IO: FLOATING; DM: sta- ble at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: FLOATING	IDD6	12			1,2,3
Self Refresh Current: Extended Temperature Range; TCASE: 0- 95°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Extended; CKE: Low; External clock: Off; CK and /CK: LOW; CL: see timing used table; BL: 8; AL: 0; /CS, Command, Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: En- abled in Mode Registers; ODT Signal: FLOATING	IDD6ET	16			2,4
Operating Bank Interleave Read Current; CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see timing used table; BL: 8; AL: CL-1; /CS: High between ACT and RDA; Com- mand, Address: partially toggling; Data IO: read data bursts with different data between one burst and the next one; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD7 (x8)	130	140	150	1,2
	IDD7 (x16)	190	200	210	1,2
RESET Low Current; RESET: Low; External clock: off; CK and /CK: LOW; CKE: FLOATING; /CS, Command, Address, Data IO: FLOATING; ODT Signal : FLOATING	IDD8	IDD2P+2mA			1,2
					1,2

NOTE :
1. Tc = 85°C; SRT and ASR are disabled.
2. Enabling ASR could increase I_{DDx} by up to an additional 2mA.
3. Restricted to Tc (MAX) = 85°C.
4. Tc = 85°C; ASR and ODT are disabled; SRT is enabled.

5 Package Outlines

Figure 7 reflects the current status of the outline dimensions of the DDR3 packages for 4Gbit components x8 configuration. For functional description of each ball see **Chapter 1.4**.

Figure 6 - Package Outline for 4Gbit Components x8 Configuration

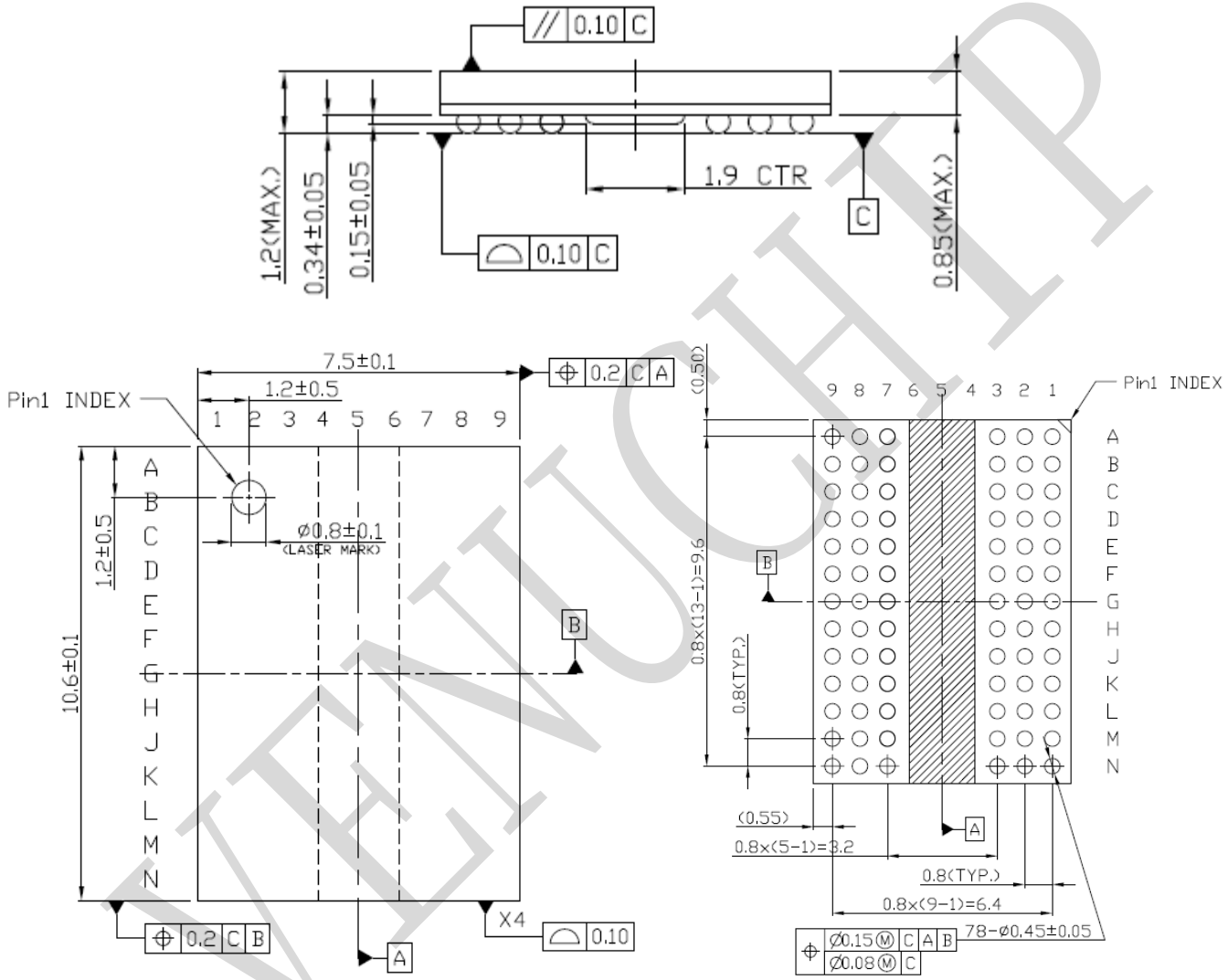
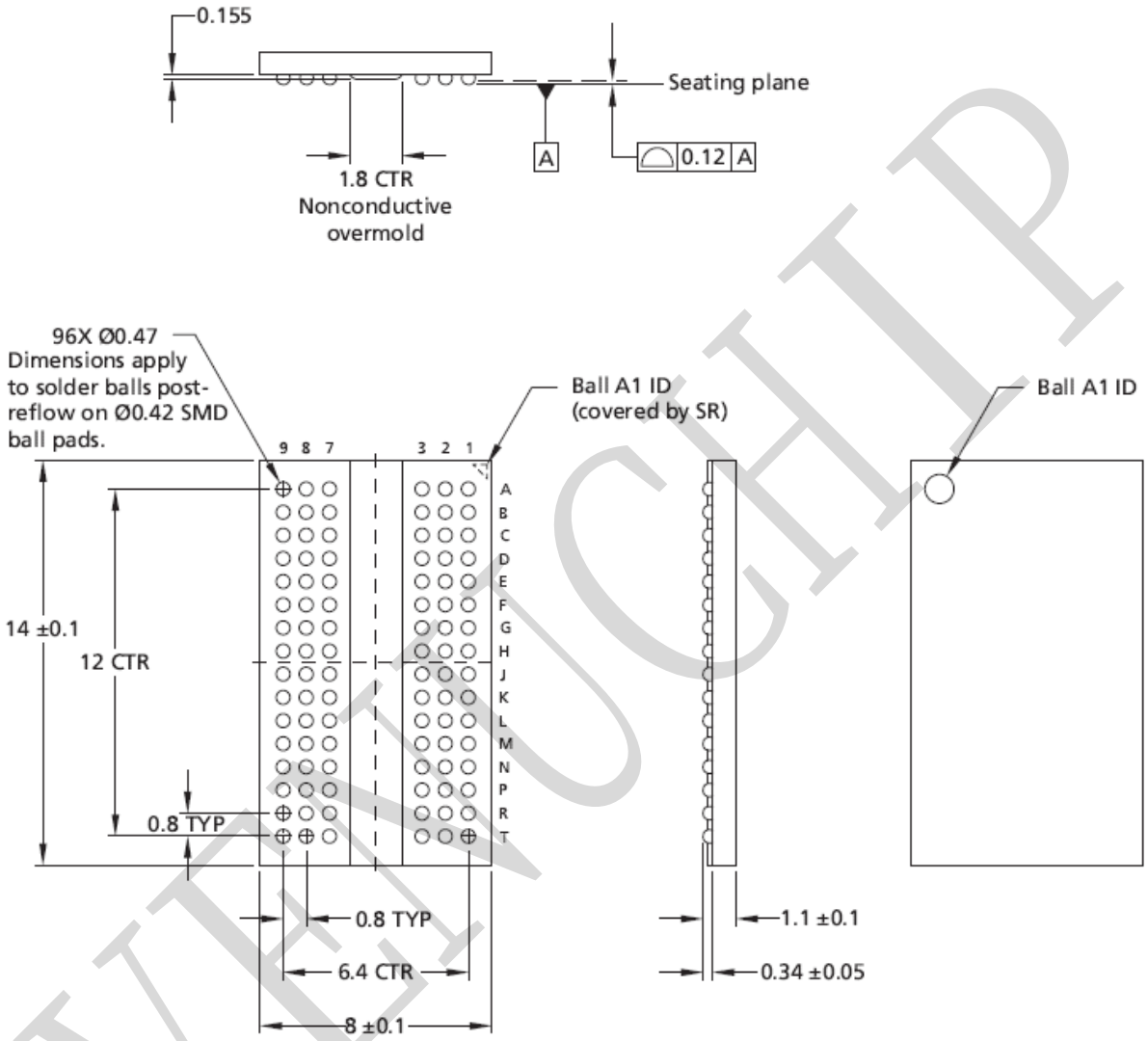


Figure 7 reflects the current status of the outline dimensions of the DDR3 packages for 4Gbit components x16 configuration. For functional description of each ball see **Chapter 1.4.**

Figure 7 - Package Outline for 4Gbit Components x16 Configuration



Notes: 1. All dimensions are in millimeters.
2. Material composition: Pb-free SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).